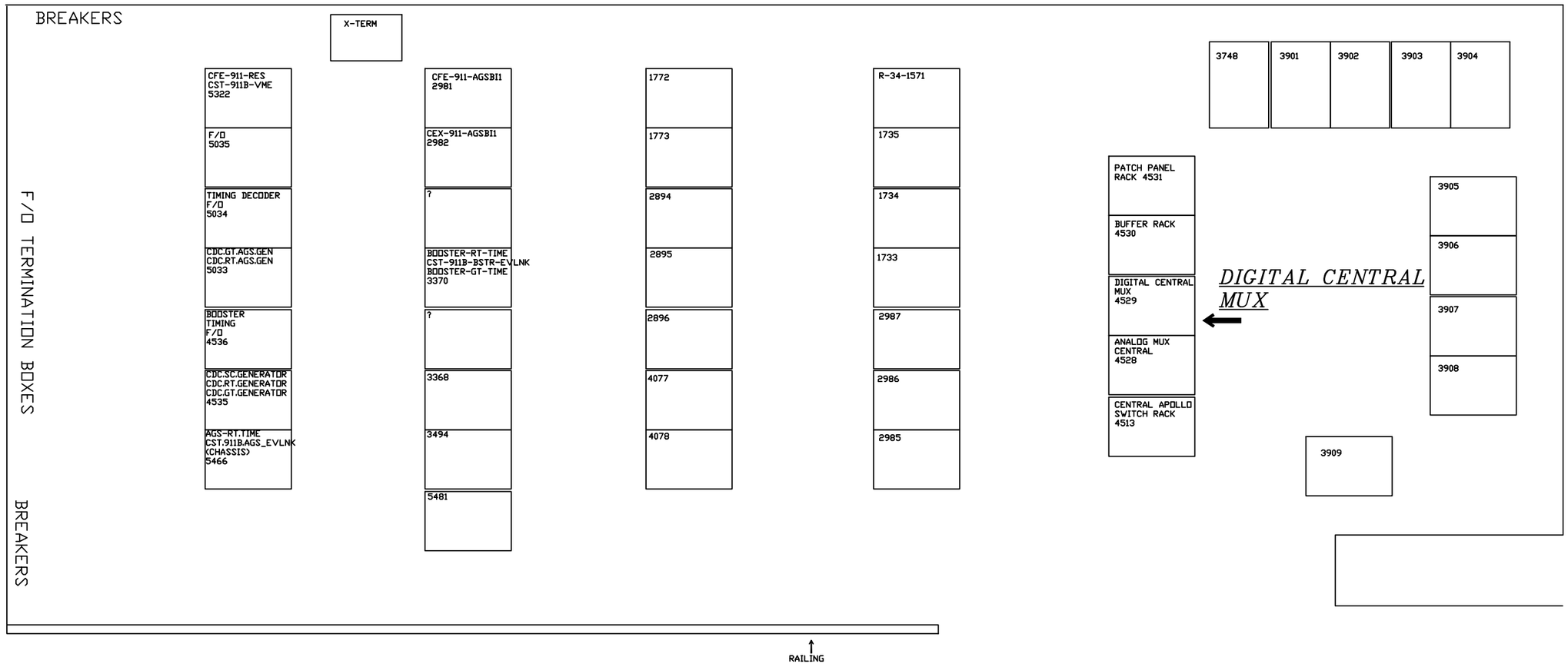


C-A Controls 5/4/01 1:27 PM 911B_floor.dwg

-3	-2	-1	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L DWG NO.,BNL NO.
QTY REQD						

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL TOLERANCES
.X ±
.XX ±
.XXX ±
ANGULAR TOLERANCE
±

OUTSTANDING ECN

NA FINISH

BREAK SHARP EDGES
MAX. XX MIN. XX

Q.A. CATEGORY		DATE
DRAWN BY	Warren Jappe	4/24/01
CHECKED BY		
DESIGN APPROVAL		
ENGINEER APPROVAL		
SUPVR. APPROVAL		

NEXT ASSEMBLY

BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973

911B FLOOR LAYOUT

SIZE | REV.
DRAWING NUMBER
MATERIAL: | SCALE: | WEIGHT: | SHEET

*AUTOCAD

CAD, CENTRAL MUX, BNL 2/16/01 2:49 PM CENTRALMUXBLOCK.dwg

REV.	ZONE	ECN NO.	DATE	BY	CKR	APP.

NOTE: INPUT SIGNALS HAVE TO BE SLOW. I USED A 2 MS PERIOD SQUARE WAVE

64 ANALOG INPUT SIGNALS

A/D MANCHESTER ENCODER CHASSIS
4 CHANNELS PER BOARD
(D36-E148 MANCHESTER ENCODER BOARD (SLOW))
UP TO 16 CARDS IN CHASSIS A

CHASSIS A RACK 4530
BLDG 911B

OUTPUT CHANNELS ON FLAT CABLE
J65 CHANNELS 1-16
J67 CHANNELS 17-32
J69 CHANNELS 33-48
J71 CHANNELS 49-64

64 ANALOG INPUT SIGNALS

A/D MANCHESTER ENCODER CHASSIS
4 CHANNELS PER BOARD
(D36-E148 MANCHESTER ENCODER BOARD (SLOW))
UP TO 16 CARDS IN CHASSIS B

CHASSIS B RACK 4530
BLDG 911B

OUTPUT CHANNELS ON FLAT CABLE
J65 CHANNELS 1-16
J67 CHANNELS 17-32
J69 CHANNELS 33-48
J71 CHANNELS 49-64

CLICK ON TO SEE SYSTEM BLOCK DIAGRAM

REF D36-E1125 F/O CABLES

6 TWINAX CABLES

BXB.930A_PS_(1-6) RK 4961
6 4X16 ANALOG MUX

F/O RECEIVER TRANSMITTER BLDG 930A RK 4932

TO BLDG 914

TO BLDG 930A

TO BLDG 930UEB

F/O RECEIVER
SLOT 3
SLOT 4
SLOT 5
SLOT 6
SLOT 7
SLOT 8
SLOT 9

14 TWINAX CABLES

PATCH PANEL IN RACK 4536

FLAT RIBBON CABLES

ANALOG BUFFER CHASSIS RK 4961

TO 930A POWER SUPPLY READBACKS
SEE VIEWMUX BXB.930A_PS_(1-6)

DIGITAL CENTRAL MUX CHASSIS

J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13 J14 J15 J16

NOT USED 4 INPUT CABLES

NOT USED 4 INPUT CABLES

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 1
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 2
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 3
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 4
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 5
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 6
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 7
SCHEMATIC D36-E70

ECL/TTL RECEIVER BD
32 INPUT CHANNELS SLOT 8
SCHEMATIC D36-E70

DIGITAL MULTIPLEXER
128 INPUT 4X8=32
OUTPUT D36-E121

U1 U2 U3 U4

INPUT 32 DIGITAL DATA LINES U1 THRU U4 TOTAL 128 DATA LINES

OUTPUT 32 DIGITAL DATA LINES

INPUT 32 DIGITAL DATA LINES

DIGITAL MULTIPLEXER
128 INPUT 4X8=32
OUTPUT D36-E121

U1 U2 U3 U4

NOT INSTALLED

ADDRESSING SWITCHES 1 2 3 4 5 6 OPEN

4 OF 32 DIGITAL DATA LINES

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 11
CONSOLE 1A,1B,1C,1D
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 12
CONSOLE 1E,1F,3A,3B
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 13
CONSOLE 3C,3D,3E,3F
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 14
CONSOLE 4A,4B,4C,4D
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 15
CONSOLE 4E,4F,5A,5B
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 16
CONSOLE 5C,5D,5E,5F
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 17
CONSOLE 6A,6B,6C,6D
SCHEMATIC D36-E124

BOOSTER DECODER 4 CHANNEL
BOARD SLOT 18
CONSOLE 6E,6F,SPARE,SPARE
SCHEMATIC D36-E124

J17 J18 J19 J20 J21 J22 J23 J24 J25 J26 J27 J28 J29 J30 J31 J32 J33 J34 J35 J36 J37 J38 J39 J40 J41 J42 J43 J44 J45 J46 J47 J48

6ea. RG58U CABLES

CYTEC MUX CHASSIS

J22 J21 J20 J19 J18 J17

J34 J33 J32 J31 J30 J29

J40 J39 J38 J37 J36 J35

J46 J45 J44 J43 J42 J41

12 INPUTS

8 OUTPUTS

12ea. RG58U CABLES

TWISTED PAIR CABLE TO CYTEC SWITCH SELECT CHASSIS

8 RIBBON CABLES

RS232C SERIAL PORT J49

CYTEC SWITCH SELECT CHASSIS

BLDG 911B RACK 5322

CST.911B.VME

TO GPIB BOARD PORT A

TCS ELECTRONICS CORP
488 FANOUT PANEL
A
J1 J2 J3 J4 J5 J6 J7 J8

488 CABLE

CDC.ANA_MUX_CENTRAL
RACK 4528 BLDG 911B
RS232C SERIAL PORT OUTPUT

488 CABLE

-3	-2	-1	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L DWG NO.,BNL NO.
QTY REQD						

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL TOLERANCES .X ± .XX ± .XXX ± ANGULAR TOLERANCE ±

NA FINISH

BREAK SHARP EDGES MAX. XX MIN. XX

OUTSTANDING ECN

Q.A. CATEGORY		DATE
DRAWN BY	Warren Jappe	2/14/01
CHECKED BY		
DESIGN APPROVAL		
ENGINEER APPROVAL		
SUPVR. APPROVAL		

NEXT ASSEMBLY

BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973

DIGITAL CENTRAL MUX SYSTEM

BLDG 911B, RACK 4529

SIZE REV. DRAWING NUMBER

MATERIAL: SCALE: WEIGHT: SHEET 2 of 5

*AUTOCAD

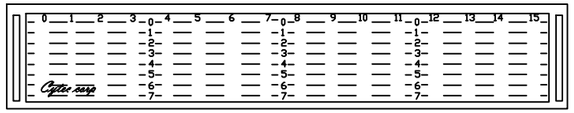
REV.	ZONE	ECN NO.	DATE	BY	CKR	APP.

SHUFFLE MUXES 8ea.

6 INPUT CHANNELS ASSIGNED TO DIGITAL CENTRAL MUX (6 through 11)

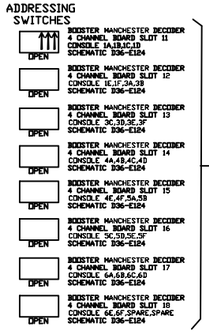
ONLY 0 TO 11 ARE USED

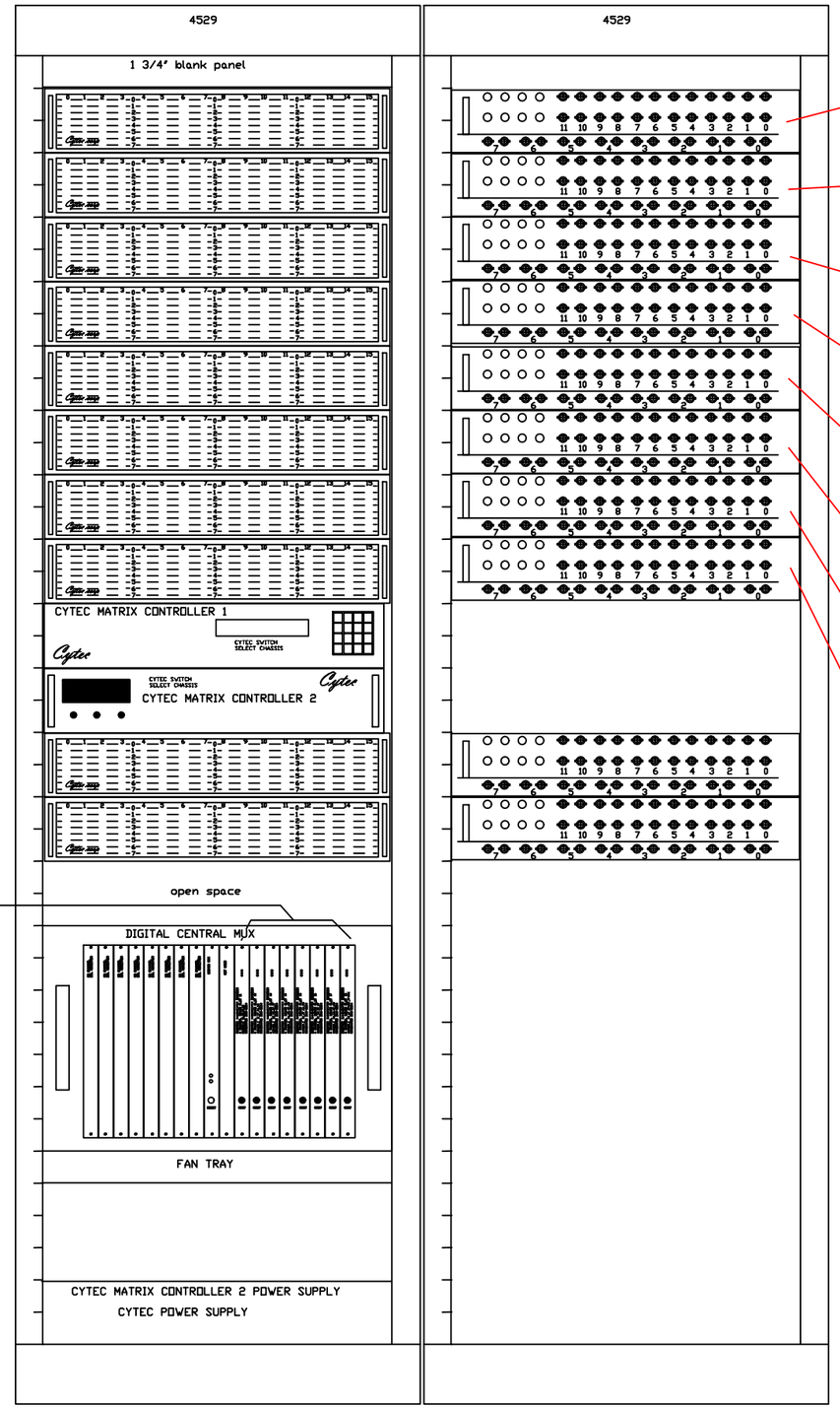
8 OUTPUT CHANNELS TO MCR SCOPES

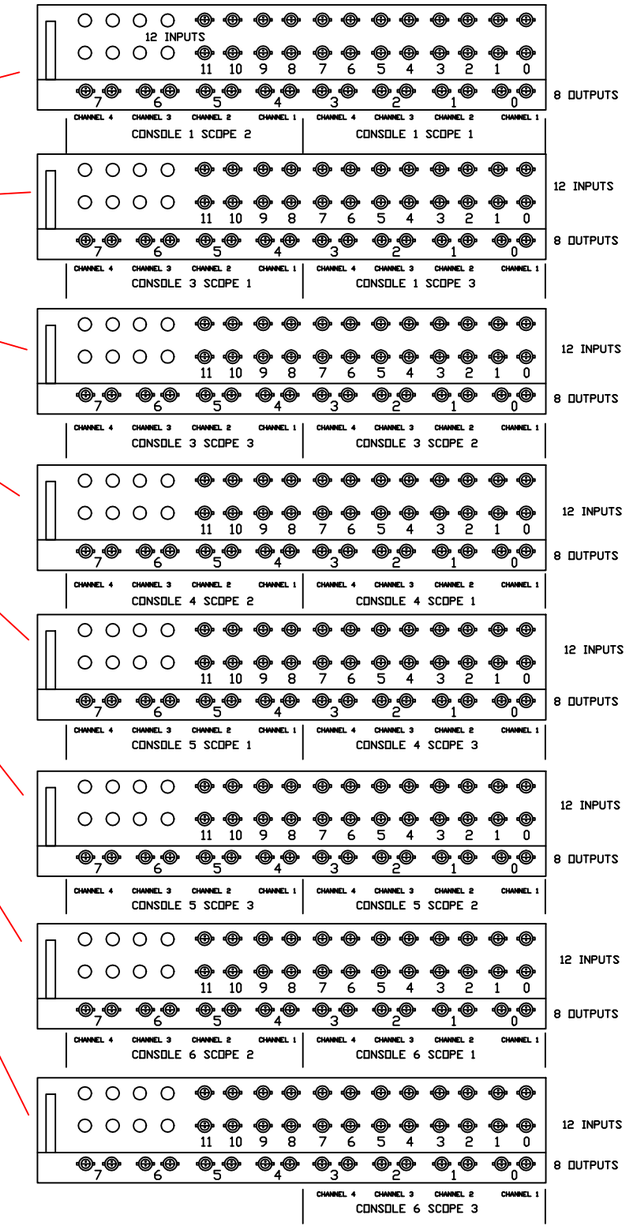


TROUBLE SHOOTING NOTE: IF MUX CANNOT SWITCH SIGNALS (ESPECIALLY AFTER A POWER DIP) NOTE THE CYTEC MATRIX CONTROLLER 2 IS IN LOCAL OR REMOTE. IT SHOULD BE IN REMOTE. IF NOT CYCLE POWER ON THE CYTEC MATRIX CONTROLLER 2 POWER SUPPLY ON THE BOTTOM OF RACK, THEN RESET THE ANALOG MUX CENTRAL CHASSIS ONE RACK TO THE LEFT (RACK 4528) THEN CHECK TO SEE IF THE LIGHT ON THE CYTEC MATRIX CONTROLLER 2 IS NOW IN REMOTE.

ADDRESSING SWITCHES







BNL, BNL 2/23/01 9:18 AM CENTMUXRACK.dwg

-3	-2	-1	QTY REQD	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L DWG NO.,BNL NO.

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL TOLERANCES .X ± .XX ± .XXX ± ANGULAR TOLERANCE ±

NA FINISH

BREAK SHARP EDGES MAX. XX MIN. XX

OUTSTANDING ECN

Q.A. CATEGORY		DATE
DRAWN BY	Warren Jappe	2/14/01
CHECKED BY		
DESIGN APPROVAL		
ENGINEER APPROVAL		
SUPVR. APPROVAL		

NEXT ASSEMBLY

BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973

DIGITAL CENTRAL MUX SYSTEM SHUFFLE MUXES

BLDG 911B RACK 4529

CONSOLE ASSIGNMENT DETAIL

SIZE REV. DRAWING NUMBER

MATERIAL: SCALE: WEIGHT: SHEET 2 of 5

1 *AUTOCAD

REV.	ZONE	ECN NO.	DATE	BY	CKR	APP.

C-A Controls, Brookhaven National Laboratory 4/2/01 2:34 PM DGTL_CENTRAL.dwg

CXB.DGTL_CENTRAL

160X32; 166 SIGNALS LISTED

LX0.RAD_MON5.A	1	84	SX0.B_TGT.B
LX0.RAD_MON5.B	2	85	SX0.C_TGT.A
LX0.XFORMERS5.A	3	86	SX0.C_TGT.B
LX0.XFORMERS5.B	4	87	SX0.BC_TGT.A
LX0.POS_MON.A	5	88	SX0.BC_TGT.B
LX0.POS_MON.B	6	89	SX0.D_TGT.A
AX0.GTR_MX1_K18.A	7	90	SX0.D_TGT.B
AX0.GTR_MX2_I18.A	8	93	SX0.B5_TGT.A
LX0.RF_AMP.A	9	94	SX0.B5_TGT.B
LX0.RF_AMP.B	10	95	SX0.F10_HOUSE.A
AX0.MISC1_EC.A	11	96	SX0.F10_HOUSE.B
AX0.MISC1_EC.B	12	97	SX0.MULTIPOLE.A
AX0.MISC1_EC.C	13	98	SX0.MULTIPOLE.B
AX0.MISC1_EC.D	14	99	SX0.SPILL_SERVO.A
AX0.A10_RLRM.A	15	100	SX0.SPILL_SERVO.B
AX0.A10_RLRM.B	16	101	AX0.GTR_MX5_A18.B
AX0.A10_RLRM.C	17	102	AX0.GTR_MX6_C18.B
AX0.A10_RLRM.D	18	103	AX0.MISC5.A
AX0.E10_RLRM.A	19	104	AX0.MISC5.B
AX0.E10_RLRM.B	20	105	AX0.INSTRU_MISC.A
AX0.MISC2_FC.A	21	106	AX0.INSTRU_MISC.B
AX0.MISC2_FC.B	22	107	AX0.SNAKE_BD921.A
AX0.MISC2_FC.C	23	108	AX0.SNAKE_BD921.B
AX0.MISC2_FC.D	24	109	ARF.RFLL.929MUX.01
AX0.MISC2_FC.E	25	110	ARF.RFLL.929MUX.02
AX0.MISC2_FC.F	26	111	ARF.RFLL.929MUX.03
AX0.MISC2_FC.G	27	112	ARF.RFLL.929MUX.04
AX0.MISC2_FC.H	28	113	BX0.914_PS_3.A
FX0.BD921_V.A	29	113	BX0.914_PS_3.B
FX0.BD921_V.B	30	113	BX0.914_PS_3.C
AX0.MISC3_IC.A	31	113	BX0.914_PS_3.D
AX0.MISC3_IC.B	32	114	BX0.914_PS_2.A
AX0.MISC3_IC.C	33	114	BX0.914_PS_2.B
AX0.MISC3_IC.D	34	114	BX0.914_PS_2.C
AX0.E10_RLRM.C	35	114	BX0.914_PS_2.D
AX0.E10_RLRM.D	36	115	BX0.914_PS_1.A
AX0.H10_RLRM.A	37	115	BX0.914_PS_1.B
AX0.H10_RLRM.B	38	115	BX0.914_PS_1.C
AX0.H10_RLRM.C	39	115	BX0.914_PS_1.D
AX0.H10_RLRM.D	40	116	BX0.914_RF_3.A
AX0.GTR_MX1_K18.B	41	116	BX0.914_RF_3.B
AX0.GTR_MX2_I18.B	42	116	BX0.914_RF_3.C
AX0.RF_VOLTS.A	43	116	BX0.914_RF_3.D
AX0.RF_VOLTS.B	44	117	BX0.914_RF_2.A
AX0.RF_VERNIER.A	45	117	BX0.914_RF_2.B
AX0.RF_VERNIER.B	46	117	BX0.914_RF_2.C
SX0.D_TGT2.A	47	117	BX0.914_RF_2.D
SX0.D_TGT2.B	48	118	BX0.914_RF_1.A
AX0.GTR_MX3_G18.B	49	118	BX0.914_RF_1.B
AX0.GTR_MX4_E10.B	50	118	BX0.914_RF_1.C
AX0.A10_HOUSE.A	51	118	BX0.914_RF_1.D
AX0.A10_HOUSE.B	52	119	BX0.930A_PS_6.A
AX0.SIEMENS.A	53	119	BX0.930A_PS_6.B
AX0.SIEMENS.B	54	119	BX0.930A_PS_6.C
AX0.SIEMENS.C	55	119	BX0.930A_PS_6.D
AX0.SIEMENS.D	56	120	BX0.930A_PS_5.A
ARI.PUE.AMUX_A2	57	120	BX0.930A_PS_5.B
ARI.PUE.AMUX_B2	58	120	BX0.930A_PS_5.C
AX0.IPM.A	59	120	BX0.930A_PS_5.D
AX0.IPM.B	60	121	BX0.930A_PS_4.A
AX0.GTR_MX3_G18.A	61	121	BX0.930A_PS_4.B
AX0.GTR_MX4_E10.A	62	121	BX0.930A_PS_4.C
AX0.RC_MUX_1.A	63	121	BX0.930A_PS_4.D
AX0.RC_MUX_1.B	64	122	BX0.930A_PS_3.A
AX0.VHF_1.A	65	122	BX0.930A_PS_3.B
AX0.VHF_1.B	66	122	BX0.930A_PS_3.C
AX0.GTR_MX5_A18.A	67	122	BX0.930A_PS_3.D
AX0.GTR_MX6_C18.A	68	123	BX0.930A_PS_2.A
AX0.RC_MUX_2.A	69	123	BX0.930A_PS_2.B
AX0.RC_MUX_2.B	70	123	BX0.930A_PS_2.C
SX0.TBH_EAST.A	71	123	BX0.930A_PS_2.D
SX0.TBH_EAST.B	72	124	BX0.930A_PS_1.A
SX0.TBH_WEST1.A	73	124	BX0.930A_PS_1.B
SX0.TBH_WEST1.B	74	124	BX0.930A_PS_1.C
SX0.TBH_WEST2.A	75	124	BX0.930A_PS_1.D
SX0.TBH_WEST2.B	76	125	BX0.930UEB_INS_2.A
SX0.MID_C1.A	77	125	BX0.930UEB_INS_2.B
SX0.MID_C1.B	78	125	BX0.930UEB_INS_2.C
SX0.MID_C2.A	79	125	BX0.930UEB_INS_2.D
SX0.MID_C2.B	80	126	BX0.930UEB_INS_1.A
SX0.A_TGT.A	81	126	BX0.930UEB_INS_1.B
SX0.A_TGT.B	82	126	BX0.930UEB_INS_1.C
SX0.B_TGT.A	83	126	BX0.930UEB_INS_1.D

CX0.DGTL_MCR_1.A	CX0.DGTL_MCR_4.E
CX0.DGTL_MCR_1.B	CX0.DGTL_MCR_4.F
CX0.DGTL_MCR_1.C	CX0.DGTL_MCR_5.A
CX0.DGTL_MCR_1.D	CX0.DGTL_MCR_5.B
CX0.DGTL_MCR_1.E	CX0.DGTL_MCR_5.C
CX0.DGTL_MCR_1.F	CX0.DGTL_MCR_5.D
CX0.DGTL_MCR_3.A	CX0.DGTL_MCR_5.E
CX0.DGTL_MCR_3.B	CX0.DGTL_MCR_5.F
CX0.DGTL_MCR_3.C	CX0.DGTL_MCR_6.A
CX0.DGTL_MCR_3.D	CX0.DGTL_MCR_6.B
CX0.DGTL_MCR_3.E	CX0.DGTL_MCR_6.C
CX0.DGTL_MCR_3.F	CX0.DGTL_MCR_6.D
CX0.DGTL_MCR_4.A	CX0.DGTL_MCR_6.E
CX0.DGTL_MCR_4.B	CX0.DGTL_MCR_6.F
CX0.DGTL_MCR_4.C	CX0.DGTL_SPARE
CX0.DGTL_MCR_4.D	CX0.DGTL_SPARE

-3	-2	-1	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L DWG NO.,BNL NO.
QTY REQD						

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL TOLERANCES
.X ±.030
.XX ±.015
.XXX ±.005
ANGULAR TOLERANCE ± .5°

OUTSTANDING ECN

NA FINISH

BREAK SHARP EDGES MAX. XX MIN. XX

Q.A. CATEGORY A-3		DATE
DRAWN BY	Jappe	4/2/2001
CHECKED BY		
DESIGN APPROVAL		
ENGINEER APPROVAL		
SUPVR. APPROVAL		

NEXT ASSEMBLY

BROOKHAVEN NATIONAL LABORATORY
ASSOCIATED UNIVERSITIES, INC.
UPTON, N.Y. 11973

Central Mux

signal block diagram

SIZE D — D09-E-RD2918 — REV. A

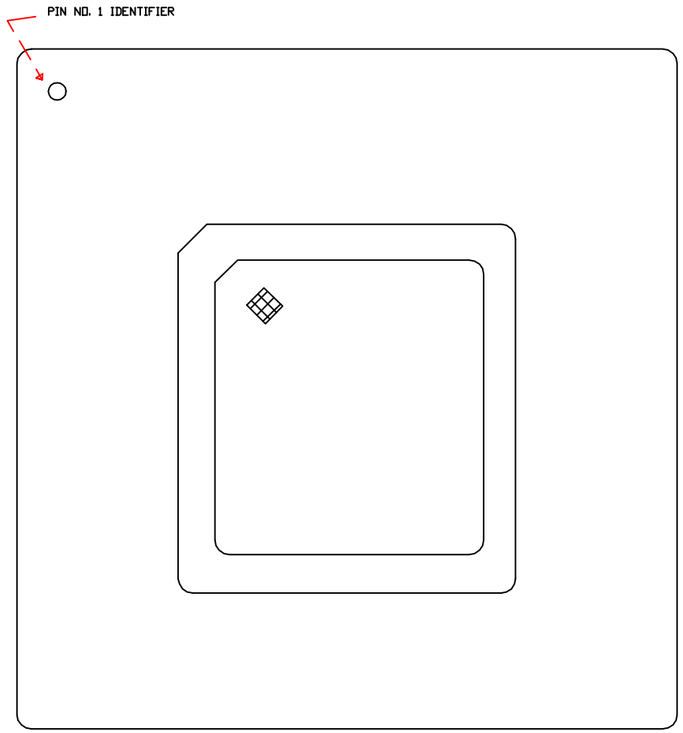
DRAWING NUMBER

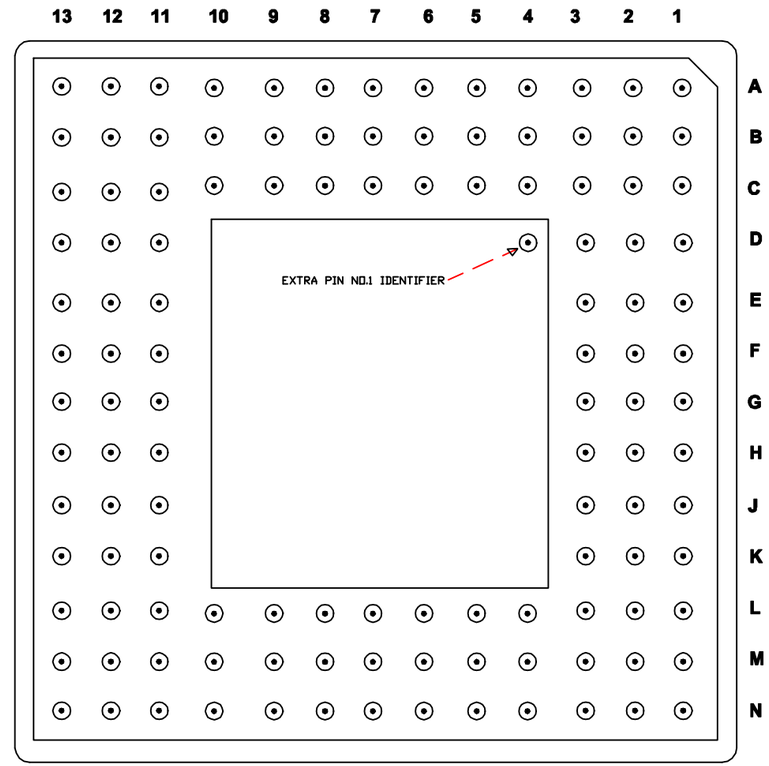
MATERIAL: ——— SCALE: FULL WEIGHT: – SHEET 3

*AUTOCAD

Package SC11320CU 121 Pin Plastic Grid Array

CONTROLS- 4/6/01 10:40 AM CENTRALMUXCHIP.dwg





REV.	ZONE	ECN NO.	DATE	BY	CKR	APP.

-3	-2	-1	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L. DWG NO.,BNL NO.
QTY REQD						

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL TOLERANCES
.X ±
.XX ±
.XXX ±
ANGULAR TOLERANCE ±

NA FINISH

BREAK SHARP EDGES
MAX. XX MIN. XX

OUTSTANDING ECN

Q.A. CATEGORY		DATE
DRAWN BY	Warren Jappe	2/14/01
CHECKED BY		
DESIGN APPROVAL		
ENGINEER APPROVAL		
SUPVR. APPROVAL		

NEXT ASSEMBLY

BROOKHAVEN NATIONAL LABORATORY
UPTON, N.Y. 11973

DIGITAL CENTRAL MUX CHIP

MUX CHIP DETAIL

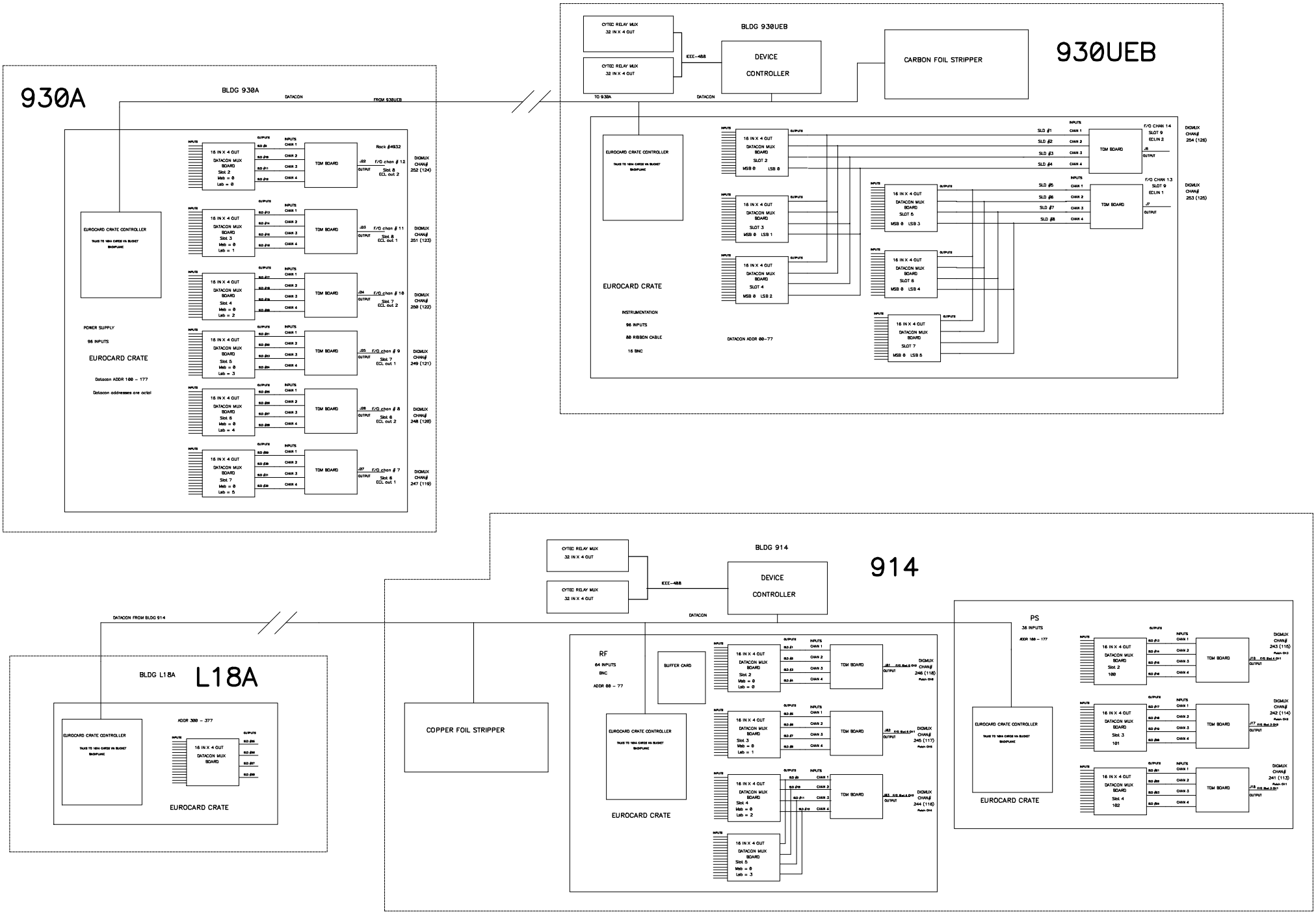
BLDG 911B, RACK 4529

SIZE | REV.

DRAWING NUMBER

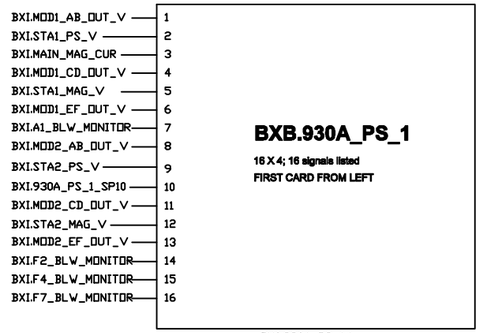
MATERIAL: | SCALE: | WEIGHT: | SHEET 2 of 5

*AUTOCAD


930A
BLDG 930A
DATACON
FROM 930UEB
EUROCARD CRATE CONTROLLER
TRUS TO 16N4 CARDS VIA BUCKET BACKPLANE
POWER SUPPLY
96 INPUTS
EUROCARD CRATE
Datacon ADDR 100 – 177
Datacon addresses are octal
16 IN X 4 OUT DATACON MUX BOARD Slot 2 Web = 0 Lab = 0
16 IN X 4 OUT DATACON MUX BOARD Slot 3 Web = 0 Lab = 1
16 IN X 4 OUT DATACON MUX BOARD Slot 4 Web = 0 Lab = 2
16 IN X 4 OUT DATACON MUX BOARD Slot 5 Web = 0 Lab = 3
16 IN X 4 OUT DATACON MUX BOARD Slot 6 Web = 0 Lab = 4
16 IN X 4 OUT DATACON MUX BOARD Slot 7 Web = 0 Lab = 5
TDM BOARD
Rack #4932
J22 F/O chan # 12 Slot 8 ECL out 2
J23 F/O chan # 11 Slot 8 ECL out 1
J24 F/O chan # 10 Slot 7 ECL out 2
J25 F/O chan # 9 Slot 7 ECL out 1
J26 F/O chan # 8 Slot 6 ECL out 2
J27 F/O chan # 7 Slot 6 ECL out 1
DIGIMUX CHAN# 252 (124)
DIGIMUX CHAN# 251 (123)
DIGIMUX CHAN# 250 (122)
DIGIMUX CHAN# 249 (121)
DIGIMUX CHAN# 248 (120)
DIGIMUX CHAN# 247 (119)
930UEB
BLDG 930UEB
CYTEC RELAY MUX 32 IN X 4 OUT
CYTEC RELAY MUX 32 IN X 4 OUT
IEEE-488
DEVICE CONTROLLER
CARBON FOIL STRIPPER
TO 930A
DATACON
EUROCARD CRATE CONTROLLER
TRUS TO 16N4 CARDS VIA BUCKET BACKPLANE
EUROCARD CRATE
INSTRUMENTATION
96 INPUTS
80 RIBBON CABLE
16 BNC
DATACON ADDR 00–77
16 IN X 4 OUT DATACON MUX BOARD SLOT 2 MSB 0 LSB 0
16 IN X 4 OUT DATACON MUX BOARD SLOT 3 MSB 0 LSB 1
16 IN X 4 OUT DATACON MUX BOARD SLOT 4 MSB 0 LSB 2
16 IN X 4 OUT DATACON MUX BOARD SLOT 5 MSB 0 LSB 3
16 IN X 4 OUT DATACON MUX BOARD SLOT 6 MSB 0 LSB 4
16 IN X 4 OUT DATACON MUX BOARD SLOT 7 MSB 0 LSB 5
SLD #1
SLD #2
SLD #3
SLD #4
SLD #5
SLD #6
SLD #7
SLD #8
F/O CHAN 14 SLOT 9 ECLIN 2
F/O CHAN 13 SLOT 9 ECLIN 1
DIGIMUX CHAN# 254 (126)
DIGIMUX CHAN# 253 (125)
L18A
BLDG L18A
DATACON FROM BLDG 914
EUROCARD CRATE CONTROLLER
TRUS TO 16N4 CARDS VIA BUCKET BACKPLANE
ADDR 300 – 377
16 IN X 4 OUT DATACON MUX BOARD
EUROCARD CRATE
914
BLDG 914
CYTEC RELAY MUX 32 IN X 4 OUT
CYTEC RELAY MUX 32 IN X 4 OUT
IEEE-488
DEVICE CONTROLLER
DATACON
COPPER FOIL STRIPPER
RF
64 INPUTS
BNC
ADDR 00 – 77
BUFFER CARD
EUROCARD CRATE CONTROLLER
TRUS TO 16N4 CARDS VIA BUCKET BACKPLANE
EUROCARD CRATE
16 IN X 4 OUT DATACON MUX BOARD Slot 2 Web = 0 Lab = 0
16 IN X 4 OUT DATACON MUX BOARD Slot 3 Web = 0 Lab = 1
16 IN X 4 OUT DATACON MUX BOARD Slot 4 Web = 0 Lab = 2
16 IN X 4 OUT DATACON MUX BOARD Slot 5 Web = 0 Lab = 3
TDM BOARD
J81 F/O Bd 0 CH3
J82 F/O Bd 0 CH1
J83 F/O Bd 0 CH2
DIGIMUX CHAN# 246 (118) Patch CH3
DIGIMUX CHAN# 245 (117) Patch CH2
DIGIMUX CHAN# 244 (116) Patch CH4
PS
36 INPUTS
ADDR 100 – 177
EUROCARD CRATE CONTROLLER
TRUS TO 16N4 CARDS VIA BUCKET BACKPLANE
EUROCARD CRATE
16 IN X 4 OUT DATACON MUX BOARD Slot 2 100
16 IN X 4 OUT DATACON MUX BOARD Slot 3 101
16 IN X 4 OUT DATACON MUX BOARD Slot 4 102
TDM BOARD
J78 F/O Bd 4 CH1
J77 F/O Bd 3 CH4
J76 F/O Bd 3 CH1
DIGIMUX CHAN# 243 (115) Patch CH3
DIGIMUX CHAN# 242 (114) Patch CH2
DIGIMUX CHAN# 241 (113) Patch CH1

CONTROLS- 4/13/01 1:49 PM fourby16.dwg

REV.	ZONE	ECN NO.	DATE	BY	CKR	APP.



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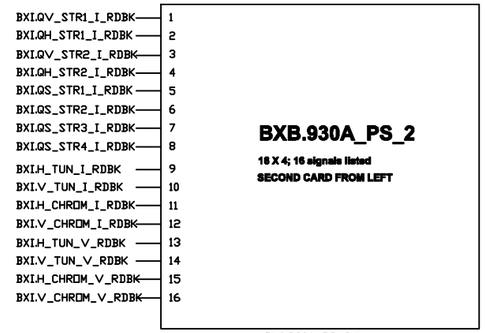

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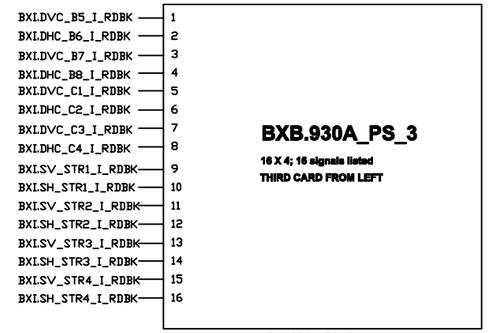

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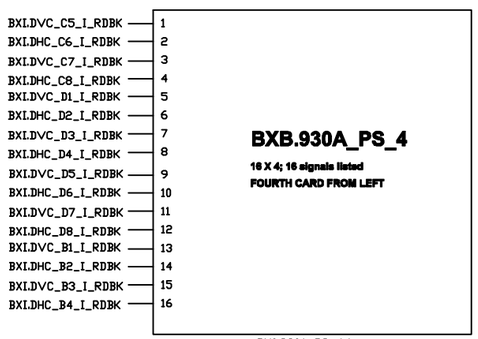

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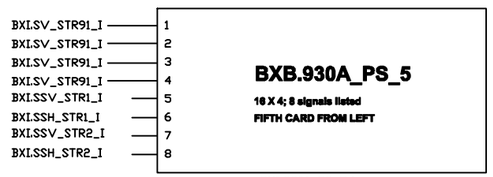

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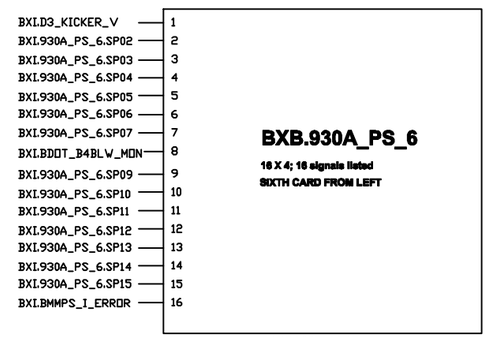


BX0.930A_PS_6.A
BX0.930A_PS_6.B
BX0.930A_PS_6.C
BX0.930A_PS_6.D

-3	-2	-1	REF DESIGNATOR	ITEM NO.	DESCRIPTION	MAT'L DWG NO.,BAL NO.
QTY REQD						

INTERPRET IN GENERAL ACCORDANCE WITH ASME Y14.24M-1989	Q.A. CATEGORY	DATE	BROOKHAVEN NATIONAL LABORATORY
	DRAWN BY: Warren Jappe	2/14/01	UPTON, N.Y. 11973
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	CHECKED BY		DIGITAL CENTRAL MUX SYSTEM
DECIMAL TOLERANCES .X ± .XX ± .XXX ± ANGULAR TOLERANCE ±	DESIGN APPROVAL		930A FIELD MUX
	ENGINEER APPROVAL		BLDG 930A, RACK 4961
	SUPVR. APPROVAL		SIZE / REV.
OUTSTANDING ECN	NA FINISH / BREAK SHARP EDGES MAX. XX MIN. XX	NEXT ASSEMBLY	DRAWING NUMBER
			MATERIAL: / SCALE: / WEIGHT: / SHEET 2 of 5

*AUTOCAD

SC11320

32 x 32 Crosspoint Switch Specification

FEATURES

- 32 x 32 Digital crosspoint structure
- CMOS technology with standby
- 50MHz operation
- CMOS compatible inputs/tri-statable outputs
- 120 pin PGA package (alternate package available)

BENEFITS

- High Density Monolithic Switch Matrix
- Low power consumption
- High performance
- Ease of interface
- High-density assembly

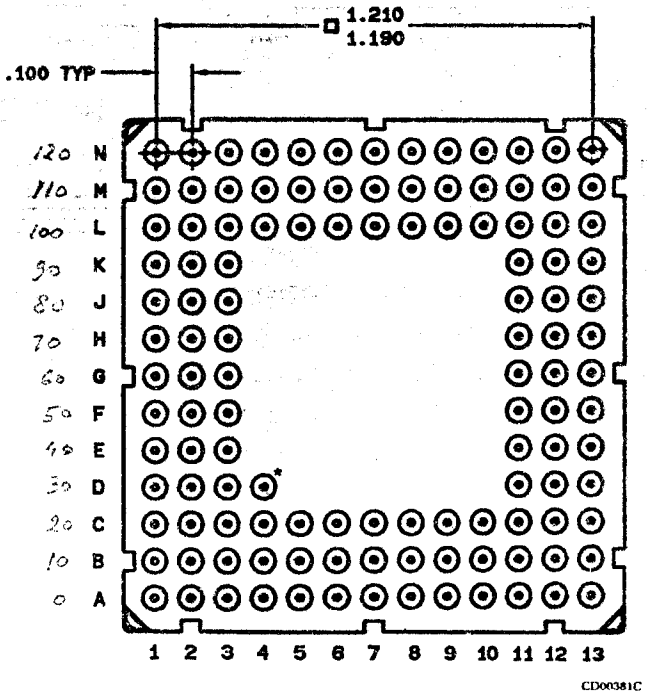
GENERAL DESCRIPTION

The 32 x 32 Crosspoint Switch is a design which allows each of the 32 outputs to be independently connected to any of its 32 inputs. Thirty-two 1 of 32 muxes are employed (each with its own register which the user loads to specify the desired input for that output channel). Outputs can also be individually tri-stated by setting bit D5 low when loading these same registers.

The block diagram of the circuit is shown in Figure 2 and should be used as a reference while reading the following sections.

PIN ASSIGNMENTS AND PIN DESCRIPTIONS

Pin Configuration (Bottom View)



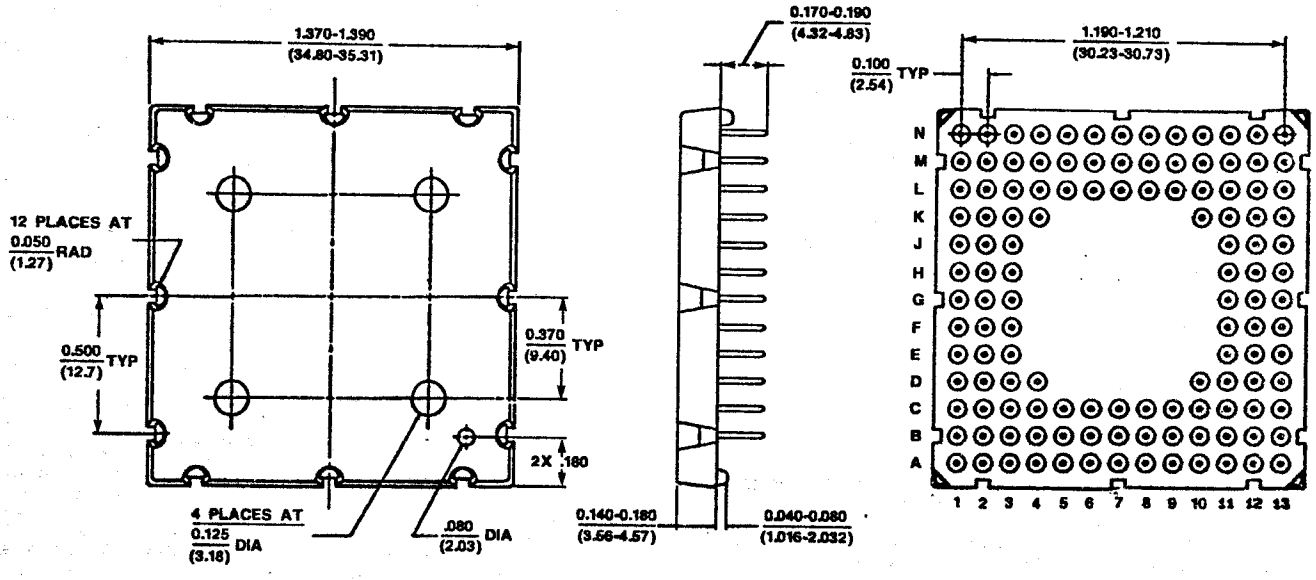
*locating pin (not electrically connected)

Order Number: SC11320CU

FIGURE 1. 120 PIN PACKAGE LAYOUT

PHYSICAL DIMENSIONS — Inches (Millimeters)

PACKAGE UP124A 124 PIN MOLDED GRID ARRAY



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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Printed in U.S.A. 011320-806

BLOCK DIAGRAM

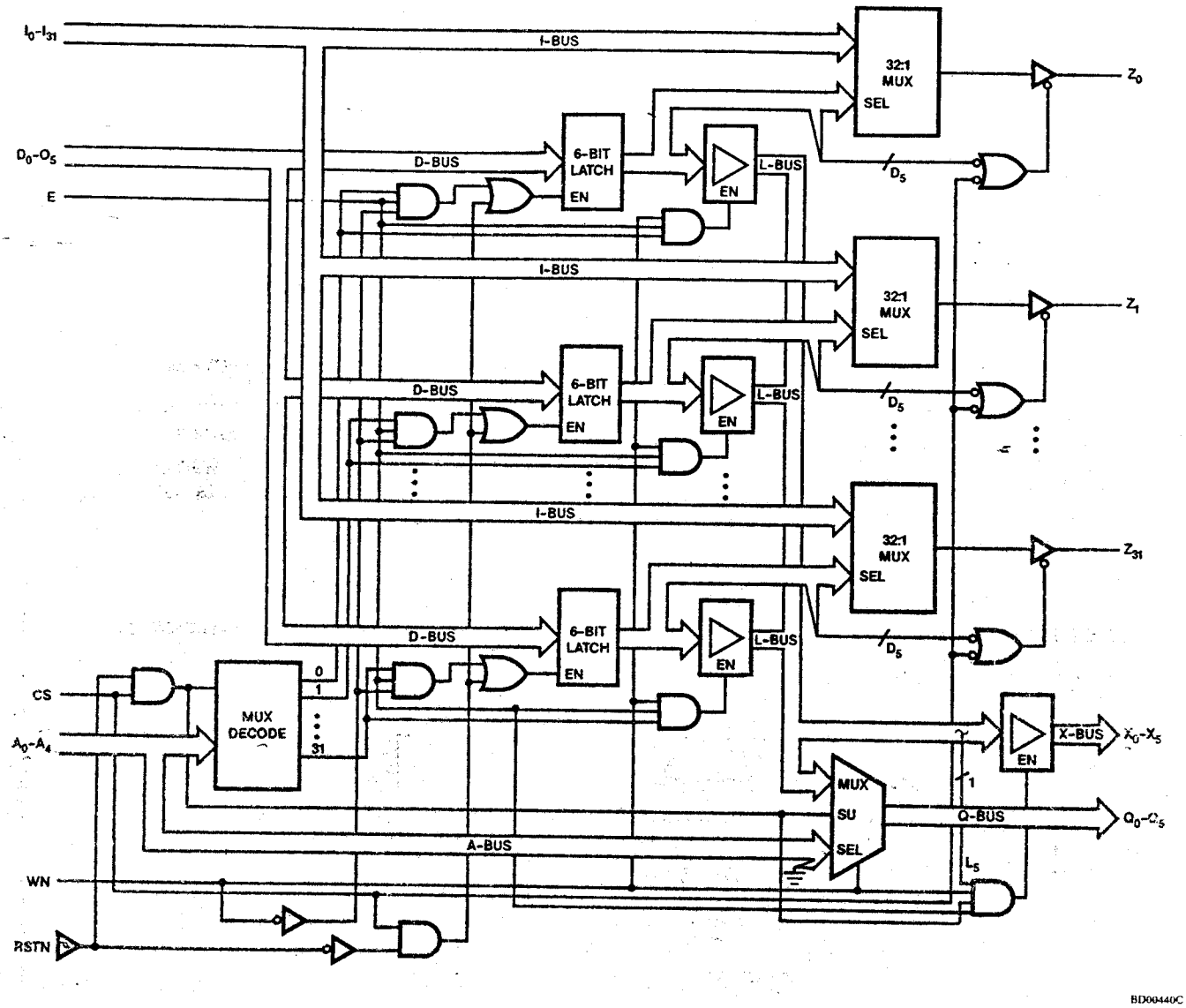

FIGURE 2. 32 x 32 CROSS-POINT SWITCH

PIN DEFINITIONS

Pin No.	Name	I/O Type	Description
1 A1	V_{SS}	Power	Pad ring ground.
13 B3	TDATA	CMOS Input	Test chain input data with internal pullup. ?
24 C4	TOUT	Output	Test chain output data.
A2	N.C.		No Connection
A3	N.C.		No Connection
14 B4	Z28	Output	Output channel (tri-state)
25 C5	Z29	Output	Output channel (tri-state)
4 A4	Z30	Output	Output channel (tri-state)
15 B5	Z31	Output	Output channel (tri-state)
A5	S0	CMOS Input	Not supported.
C6	S1	CMOS Input	Not supported.
B6	S2	CMOS Input	Not supported.
A6	S3	CMOS Input	Not supported.
A7	S4	CMOS Input	~~Select address for mux monitor~~. ?
27 C7	V_{DD}	Power	Internal logic +5.0 VDC
17 B7	V_{SS}	Power	Internal logic ground
A8	MZ	Output	Not supported. ?
18 B8	D0	CMOS Input	Mux register input data (write operation).
38 C8	D1	CMOS Input	Mux register input data (write operation).
9 A9	D2	CMOS Input	Mux register input data (write operation).
19 B9	D3	CMOS Input	Mux register input data (write operation).
10 A10	D4	CMOS Input	Mux register input data (write operation).
29 C9	D5	CMOS Input	Register data for output tri-state control.
20 B10	I0	CMOS Input	Channel input data.
11 A11	Z0	Output	Output channel (tri-state).
21 B11	Z1	Output	Output channel (tri-state).
30 C10	Z2	Output	Output channel (tri-state).
12 A12	Z3	Output	Output channel (tri-state).
B12	N.C.		No Connection
31 C11	V_{SS}	Power	Pad ring ground
13 A13	V_{DD}	Power	Pad ring +5.0 VDC
32 C12	I1	CMOS Input	Channel input data.
41 D11	I2	CMOS Input	Channel input data.
23 B13	I3	CMOS Input	Channel input data.
33 C13	I4	CMOS Input	Channel input data.
42 D12	I5	CMOS Input	Channel input data.
51 E11	I6	CMOS Input	Channel input data.
43 D13	I7	CMOS Input	Channel input data.
52 E12	Z4	Output	Channel output (tri-state).
53 E13	Z5	Output	Channel output (tri-state).
61 F11	Z6	Output	Channel output (tri-state).

A 0
B 10
C 20
D 30
E 40
F 50
G 60
H 70
J 80
K 90
L 100
M 110
N 120

PIN DEFINITIONS

Pin No.	Name	I/O Type	Description
62 F12	Z7	Output	Channel output (tri-state).
63 F13	Z8	Output	Channel output (tri-state).
73 G13	V_{SS}	Power	Pad ring ground
71 G11	V_{SS}	Power	Pad ring ground
72 G12	V_{DD}	Power	Pad ring +5.0 VDC
83 H13	Z9	Output	Channel output (tri-state).
82 H12	Z10	Output	Channel output (tri-state).
81 H11	Z11	Output	Channel output (tri-state).
93 J13	Z12	Output	Channel output (tri-state).
92 J12	Z13	Output	Channel output (tri-state).
103 K13	I8	CMOS Input	Channel input data.
91 J11	I9	CMOS Input	Channel input data.
102 K12	I10	CMOS Input	Channel input data.
113 L13	I11	CMOS Input	Channel input data.
112 L12	I12	CMOS Input	Channel input data.
101 K11	I13	CMOS Input	Channel input data.
123 M13	I14	CMOS Input	Channel input data.
122 M12	I15	CMOS Input	Channel input data.
111 L11	V_{DD}	Power	Pad ring +5.0 VDC
133 N13	V_{SS}	Power	Pad ring ground
121 M11	X5	Output	Bit 5 of L-Bus (tri-state).
110 L10	Z14	Output	Channel output (tri-state).
132 N12	Z15	Output	Channel output (tri-state).
131 N11	Z16	Output	Channel output (tri-state).
120 M10	Z17	Output	Channel output (tri-state).
109 L9	I16	CMOS Input	Channel input data.
130 N10	I17	CMOS Input	Channel input data.
119 M9	A0	CMOS Input	Address for channel mux selection.
129 N9	A1	CMOS Input	Address for channel mux selection.
108 L8	A2	CMOS Input	Address for channel mux selection.
118 M8	A3	CMOS Input	Address for channel mux selection.
128 N8	A4	CMOS Input	Address for channel mux selection.
127 N7	V_{DD}	Power	Internal logic +5.0 VDC
107 L7	X0	Output	Bit 0 of L-Bus (tri-state).
117 M7	V_{SS}	Power	Internal logic ground
126 N6	E	CMOS Input	Enable. Active high enable for read and write operations.
116 M6	WN	CMOS Input	Write Not. Active low write strobe.
106 L6	RSTN	CMOS Input	Reset Not. Active low chip reset. (Schmitt trigger input)
125 N5	CS	CMOS Input	Chip Select. Active high enable for all operations. (Z and X outputs float when CS is low.)

A 0
B 10
C 20
D 30
E 40
F 50
G 60
H 70
J 80
K 90
L 100
M 110
N 120

PIN DEFINITIONS

Pin No.	Name	I/O Type	Description
115 M5	Q0	Output	L-Bus contents (read operation) / A-Bus contents (write operation)
124 N4	Q1	Output	
105 L5	Q2	Output	
114 M4	Q3	Output	
123 N3	Q4	Output	
113 M3	Q5	Output	Mux register output data (read operation).
104 L4	X1	Output	Bit 1 of L-Bus (tri-state).
122 N2	X2	Output	Bit 2 of L-Bus (tri-state).
112 M2	X3	Output	Bit 3 of L-Bus (tri-state).
103 L3	V_{SS}	Power	Pad ring ground
121 N1	V_{DD}	Power	Pad ring +5.0 VDC
102 L2	X4	Output	Bit 4 of L-Bus (tri-state).
93 K3	I18	CMOS Input	Channel input data.
111 M1	I19	CMOS Input	Channel input data.
101 L1	I20	CMOS Input	Channel input data.
92 K2	I21	CMOS Input	Channel input data.
83 J3	I22	CMOS Input	Channel input data.
91 K1	I23	CMOS Input	Channel input data.
82 J2	Z18	Output	Channel output (tri-state).
81 J1	Z19	Output	Channel output (tri-state).
73 H3	Z20	Output	Channel output (tri-state).
72 H2	Z21	Output	Channel output (tri-state).
71 H1	Z22	Output	Channel output (tri-state).
61 G1	V_{SS}	Power	Pad ring ground
63 G3	V_{SS}	Power	Pad ring ground
62 G2	V_{DD}	Power	Pad ring +5.0 VDC
51 F1	Z23	Output	Channel output (tri-state).
52 F2	Z24	Output	Channel output (tri-state).
53 F3	Z25	Output	Channel output (tri-state).
41 E1	Z26	Output	Channel output (tri-state).
42 E2	Z27	Output	Channel output (tri-state).
31 D1	I24	CMOS Input	Channel input data.
43 E3	I25	CMOS Input	Channel input data.
32 D2	I26	CMOS Input	Channel input data.
21 C1	I27	CMOS Input	Channel input data.
22 C2	I28	CMOS Input	Channel input data.
33 D3	I29	CMOS Input	Channel input data.
11 B1	I30	CMOS Input	Channel input data.
12 B2	I31	CMOS Input	Channel input data.
23 C3	V_{DD}	Power	Pad ring

Overview

As a 32 x 32 cross-point switch, this IC's primary mission is to allow a user to independently connect any of 32 inputs to one of its 32 outputs. The circuit must also support applications where multiple switches are placed in parallel (outputs wired-ored together) to create even larger systems.

Structure

To provide the flexible switching behavior required (no inputs blocking), 32 muxes are used (one for each output). Each of these muxes is a 32:1 type as there are 32 input channels to choose from. A six bit latch is also provided for every mux to allow the user to individually load the desired input address for each output channel. Five of the six latch bits (D0-D4) are for describing the mux input while bit D5 is reserved for enabling the channel's output driver (0 = tri-state, 1 = driving). As the host needs to update a mux's latch without interfering with the other outputs, a decoder using five address lines as inputs is included. To enhance in-circuit testability, the outputs of all 32 six bit latches are wire-ored to form the L-bus which can be read by the host on the X-Bus tri-statable outputs. Another diagnostic output bus (the Q-Bus) can relay the status of both the L-Bus and the A-Bus (WN = 0: A-Bus, WN = 1: L-Bus), but cannot be tri-stated.

A summary of the circuit's behavior is presented in a truth table format (Figure 3). A detailed discussion of the various operational modes follows.

		READ MODE	WRITE MODE	IDLE MODE	RESET MODE	UNSELECT MODE
IN	CS	H	H	H	X*	L
	RSTN	H	H	H	L	X
	E	H	H	L	X	X
	WN	H	L	X	X	X
OUT	Q-Bus	D0-D5	A0-A4, Q5 = 0	L	L	L
	X-Bus	D0-D5**	Hi-Z	Hi-Z	Hi-Z	Hi-Z
	Z-Bus	Respective selected input**				Hi-Z

(*) Don't Care
(**) if D5 = 1, else Hi-Z

FIGURE 3. TRUTH TABLE

Unselected Mode

As Figure 3 suggests, the chip immediately enters the unselected mode when CS is taken low (regardless of the other control inputs). In this state, the Q-Bus outputs go low while the Z-Bus and X-Bus float. The contents of the mux latches are not affected.

Reset Mode

In the case where RSTN = 0, the reset mode begins. Here, all the mux latches are enabled at once (NOT CLEARED!). Depending on CS and the contents of the D-Bus, the Z-Bus outputs will either all reflect the state of the input specified (CS and D5 = 1) or all be floating (CS or D5 = 0). To clear the mux latches, the host must assure the presence of low inputs on the D-Bus before and after the RSTN line is brought high. For in-circuit testing, the host can use this mode to exercise all 32 muxes simultaneously. Both the Q-Bus and X-Bus outputs are inactive while RSTN is low. A Schmitt trigger input is provided for RSTN to support the slow rise times seen when external capacitance is used for holding RSTN low during power-up.

Idle Mode

The idle mode is encountered when both CS and RSTN are high but E is low. In this case, each mux uses the previously stored contents of its latch to choose an input to pass to its output. The Z-Bus drivers are enabled (subject to D5 as discussed previously) while the Q-Bus and X-Bus are inactive.

Write Mode

To modify the contents of a single mux's latch, the WN line must be low while CS, RSTN, and E are all high. The latch selected by the A-Bus is immediately loaded with the contents of the D-Bus and this information is latched by the rising edge of the WN line. While WN is low, the Q-Bus outputs the contents of the A-Bus (A0-A4 on lines Q0-Q4, Q5 always low). It should be noted that only the selected mux's output can change during a write cycle. This insures that the other output channels can continue to pass their data independently of the operation.

Read Mode

When all four of the control lines (CS, RSTN, E, WN) are high, the chip is in the read mode. During this time, the X-Bus reflects the contents of the L-Bus if L5 is high, otherwise the X-Bus floats. Meanwhile, the Q-Bus also displays the L-Bus status but without regard to L5.

DC OPERATING CONDITIONS

Description	Min	Typ	Max	Units	Notes
Operating Ambient Air Temperature Range	0	25	70	°C	junction range 0 to 85
Power Supplies					
V_{DD} Supply Voltage	4.5	5.0	5.5	V	
V_{ss} Supply Voltage	0	0	0	V	
I_{DD} Supply Current			170	mA	20MHz
Leakage Current (all inputs & tri-state outputs)	−10		+10	μA	
Input Voltages					
Logic "0" (V_{IL}) all except RSTN			1.5	V	
Logic "1" (V_{IH}) all except RSTN	3.5			V	
Logic "0" (V_{IL}) RSTN only	1.3	1.8	2.0	V	
Logic "1" (V_{IH}) RSTN only	3.0	3.5	3.8	V	
Schmitt Trigger Hysteresis	1.0	1.7	2.0	V	
Output Voltages					
Z0-Z31					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +8mA
Logic "1" (V_{OH})	V_{DD}-0.8		V_{DD}	V	I_{OH} = −8mA
X0-X5, Q0-Q5					
Logic "0" (V_{OL})	V_{SS}		0.8	V	I_{OL} = +4mA
Logic "1" (V_{OH})	V_{DD}-0.8		V_{DD}	V	I_{OH} = −4mA
Input Capacitance			10	pF	w/package
Output Capacitance			10	pF	w/package
Output Loading					
Q0-Q5			20	pF	
Z0-Z31			50	pF	
X0-X5			170	pF	

AC CHARACTERISTICS (Refer to Figures 4.1 thru 4.5)
(@ $V_{DD} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_A = 0$ to 70°C. Outputs loaded and timing measured at CMOS levels. All input rise and fall times < 10ns, unless otherwise specified)

Symbol	Description	Min	Typ	Max	Units	Notes
t1	I-Bus Rise Time			5	nS	Figure 4.1 (symmetry: 50/50 in 45/55 out at 50MHz)
t2	I-Bus Fall Time			5	nS	
t3	Propagation Time (Rising)			40	ns	
t4	Propagation Time (Falling)			40	ns	
t5	Z-Bus Rise Time	4		11	nS	(with 50pF load on Z-Bus)
t6	Z-Bus Fall Time	4		11	nS	
	I-Bus Frequency			50	MHz	
t7	Reset Fall to Z-Bus Change			55	nS	
t7b	Reset Pulse Width	100			nS	
t8	D-Bus Hold From Reset Rise	20			nS	Figure 4.2
t9	D-Bus to Z-Bus Delay			40	nS	
t10	CS Fall to Z-Bus Float			25	nS	
t11	CS Rise to Z-Bus Driven			25	nS	(if D5 = 1) Figure 4.3
t12	CS FALL to X-Bus Float			30	nS	
t13	CS Rise to X-Bus Driven			30	nS	(if D5 = 1)
t14	CS Fall to Q-Bus Low			40	nS	
t15	CS Rise to Q-Bus Enabled			50	nS	
t16	A-Bus Setup Before E Rise	50			nS	
t17	A-Bus Hold After E Fall	20			nS	Figure 4.4
t18	WN Setup Before E Rise	50			nS	
t19	WN Hold After E Fall	20			nS	
t20	D-Bus Setup Before E Rise	50			nS	
t21	D-Bus Hold After E Fall	20			nS	
t22	WN Rise to Zx Change			85	nS	
t23	E Rise to Q-Bus Active			40	nS	(A0-A4, 0)
t24	E Fall to Q-Bus Low			35	nS	
t24b	E Pulse Width	20			nS	
t25	A-Bus Setup Before E Rise	50			nS	
t26	A-Bus Hold After E Fall	50			nS	Figure 4.5
t27	WN Setup Before E Rise	50			nS	
t28	WN Hold After E Fall	20			nS	
t29	E Rise to Q-Bus Active			55	nS	(L0-L5)
t30	E Fall to Q-Bus Low			35	nS	
t31	E Rise to X-Bus Active			85	nS	(L0-L5)
t32	E Fall to X-Bus Float			30	nS	

MECHANICAL SPECIFICATIONS

Package

121 pin grid array (plastic, one locating pin)

TIMING DIAGRAMS

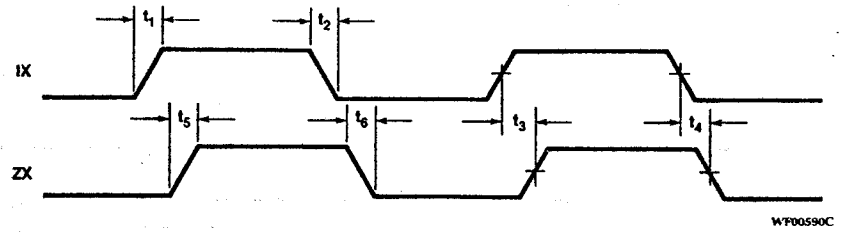

FIGURE 4.1. IDLE

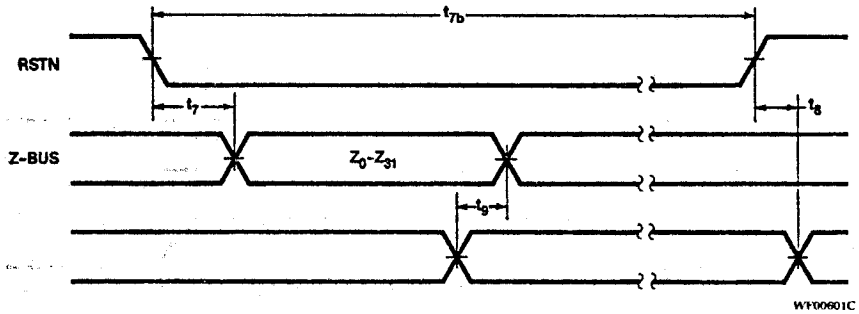

FIGURE 4.2. RESET

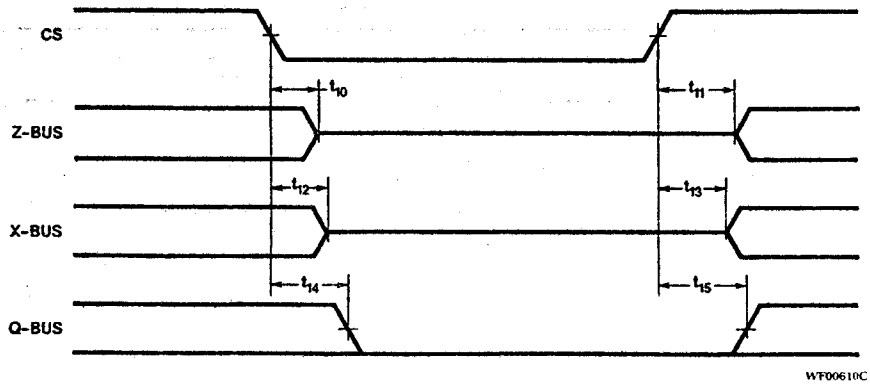

FIGURE 4.3. UNSELECT

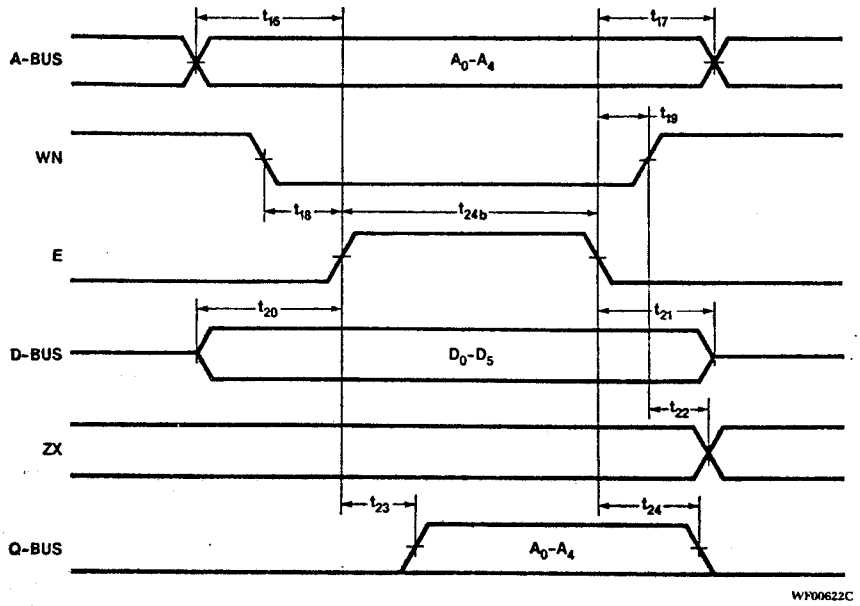

FIGURE 4.4. WRITE

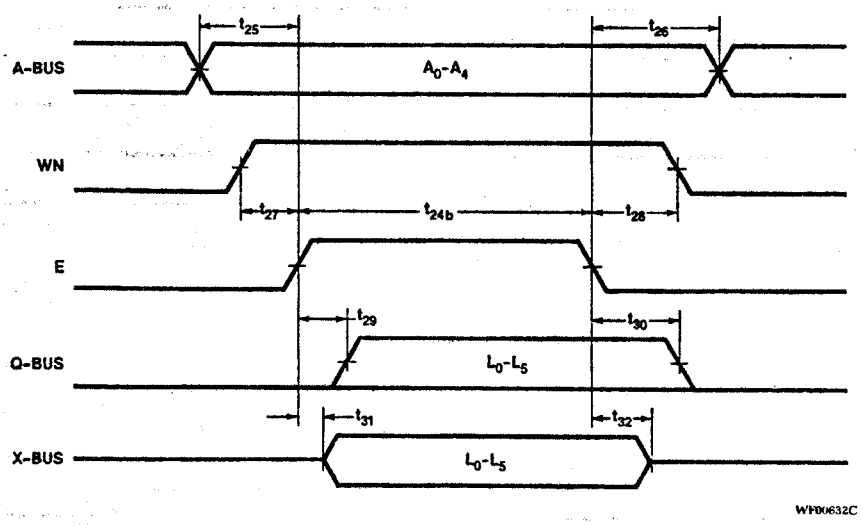

FIGURE 4.5. READ

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SIERRA SEMICONDUCTOR
2075 No. Capitol Ave.
San Jose, CA 95132
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FAX:408-263-3337

Air Market Bill Nicholson

Northwest Regional Office
(Same as Headquarters)

N. Central Regional Office
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1420 Kensington Rd., Ste. 208
Oak Brook, IL 60521
PH: 312-573-1331
FAX: 312-573-1354

Southwest Regional Office
SIERRA SEMICONDUCTOR
17870 Sky Park Circle Ste. 107
Irvine, CA 92714-6242
PH: 714-261-5707
FAX: 714-261-2738

DESIGN CENTER LOCATION
— Corporate Headquarters
— N. Central Regional Office
— Northeast Regional Office

Northeast Regional Office
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Burlington, MA 01803
PH: 617-229-6868
FAX: 617-229-6849

S. Central Regional Office
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801 E. Campbell Rd., Ste. 255
Richardson, TX 75081
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FAX: 214-680-2271

Southeast Regional Office
SIERRA SEMICONDUCTOR
Palms Office Center, Ste. 38
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Melbourne, FL 32935
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FAX: 407-259-2518

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4922-B Cotton Row
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FAX: 205-837-7049

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6016 E. Larkspur
Scottsdale, AZ 85254
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FAX: 918-492-8781

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FAX: 203-266-0784

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FAX: 301-992-5846

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Deerfield Beach, FL 33442-3025
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FAX: 305-427-7338

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THE MCCOY GROUP
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FAX: 609-953-1238

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2002 Teall Ave.
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Eastern Penn.
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FAX: 416-675-6871

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Nepean, Ontario K2H 8R2
Canada
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FAX: 613-726-8834

ELECTRO SOURCE, INC.
6600 Trans Canada Hwy;
Ste. 510
Pointe Claire, Quebec H9R 4S2
Canada
PH: 514-694-0404
FAX: 514-694-8501

RLRM CYTEC MUX H10, E10, A10

CH0 ----DB37 PIN 35
CH1 ----DB37 PIN 34
CH2 ----DB37 PIN 33
CH3 ----DB37 PIN 32
CH4 ----DB37 PIN 31
CH5 ----DB37 PIN 30
CH6 ----DB37 PIN 29
CH7 ----DB37 PIN 28
CH8 ----DB37 PIN 27
CH9 ----DB37 PIN 26
CH10 ---DB37 PIN 25
CH11 ---DB37 PIN 24
CH12 ---DB37 PIN 23
CH13 ---DB37 PIN 22
CH14 ---DB37 PIN 21
CH15 ---DB37 PIN 20
CH16 ---DB37 PIN 1
CH17 ---DB37 PIN 2
CH18 ---DB37 PIN 3
CH19 ---DB37 PIN 4
CH20 ---DB37 PIN 5
CH21 ---DB37 PIN 6
CH22 ---DB37 PIN 7
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CH25 ---DB37 PIN 10
CH26 ---DB37 PIN 11
CH27 ---DB37 PIN 12
CH28 ---DB37 PIN 13
CH29 ---DB37 PIN 14
CH30 ---DB37 PIN 15
CH31 ---DB37 PIN 16
Common----DB37 PIN 17, 18, 19, 36, 37