

BROOKHAVEN NATIONAL LABORATORY
RELATIVISTIC HEAVY ION COLLIDER CONTROLS

POWER SUPPLY WAVEFORM GENERATOR (V115)
ACCEPTANCE TEST PROCEDURE
REV. D

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Prepared by: Tim Kahn

Supervisor:

Revision Validation Table

test procedure revision	V115 revision	date	enr	supervisor
A	A, B	4/25/95	T. K.	
B	A,B,C	2/26/97	Tom K	
C	A,B,C,D	8/15/97	Tom K	
D	A,B,C,D,E	7/22/98	Tom K	

This test procedure is valid only for V115 with revision letter registered in the validation table.

File Name=H:\kahn\ramp_gen.b\doc\test_pro.doc

2/26/97-Changed to Rev. B to add V115 Rev. C in validation table. Deleted steps 3 to 8 under power on, removed steps to power on and off when removing jumpers under manual test. Added jumper list and programming info.

Ed Koropsak

8/15/97-Changed to Rev. C to add V115 Rev. D in validation table and add test error codes.

7/22/98-Changed to Rev D to add V115 Rev. E in validation table and to add T115/T215 testing.

8/11/99-Corrected typo's and operations file names.

PREFIX

The Waveform Generator (V115) Acceptance Test shall be performed by the qualified personnel. The procedure shall be strictly followed to carry out the complete test. The test record shall be shipped along with UUT (Unit Under Test). For BNL ACS personnel, the record shall be filed in the QA log.

TEST STATION SETUP:

- 1 Setup Waveform Generator Test Station as shown in figure 1.
- 2 Setup Windows Terminal by open terminal configuration file WFG_TEST.TRM.

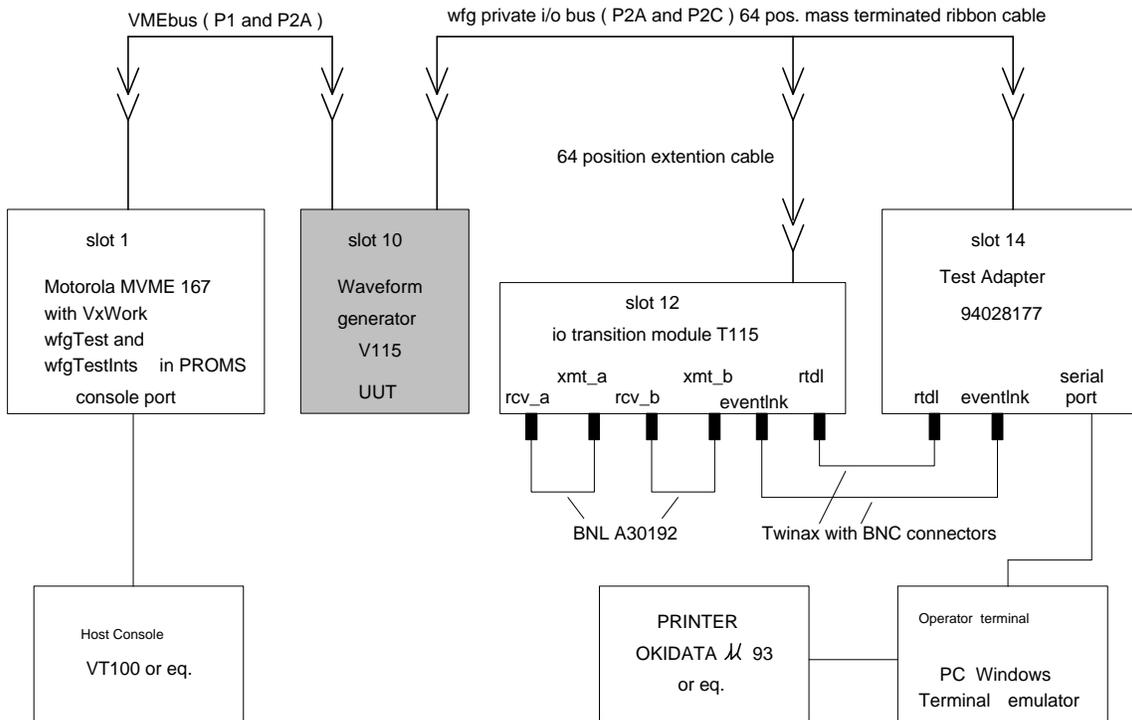


Figure 1

V115 Acceptance Test Record

UUT PREPARATION:

- 1 Enter UUT revision letter here: ()
- 2 Verify that UUT's revision is shown on this procedure's validation table. ()
- 3 Enter UUT serial number. ()
- 4 Verify the QA record to confirm that incoming inspection has been done to UUT. ()
- 5 Using multi-meters to verify that NO SHORTS across the two leads of C4,
and that NO SHORTS across the leads of C7 ()
- 6 Verify that the jumpers are installed per default jumper list on drawing 94028106 . ()

POWER-ON AND INITIALIZATION:

- 1 Remove all address jumpers at JB1.
Install UUT in slot 10 as shown in figure 1.
- 2 Turn on power on the test station(VME crate.)
- 3 On the host console, at prompt (=>) enter:
wfgFlash("/home/cfsa/kahn/wfgtest/image","/dev/wfg")
- 4 Wait for the test code to be downloaded .
- 5 On the host console, Verify that no error is reported. ()

MANUAL TEST

- 1 On the host console, enter "D 0xf0000000,64,1"
- 2 Verify that VME light blinks. ()
- 3 On the host console, verify that UUT board ID string is displayed:
* . V . M . E . I . D . B . N . L *
* . V . 1 . 1 . 5 *
* . . E . x . x . x . x . x . x *
* * where x's is serial number
- 4 Verify that the serial number matches UUT's serial number ()
- 5 Remove jumper from JB1-6 to JB1-7 on UUT
- 6
- 7 On the host console, enter "D 0xf0040000,64,1"
- 8 Verify that VME light blinks, and that UUT board ID string is displayed: ()
- 9 Remove jumper from JB1-5 to JB1-8 on UUT.
- 10 On the host console, enter "D 0xf00c0000,64,1"
- 11 Verify that VME light blinks, and that UUT board ID string is displayed: ()
- 12 Remove jumper from JB1-4 to JB1-9 on UUT.
- 13 On the host console, enter "D 0xf01c0000,64,1"
- 14 Verify that VME light blinks, and that UUT board ID string is displayed: ()
- 15 Remove jumper from JB1-3 to JB1-10 on UUT.
- 16 On the host console, enter "D 0xf03c0000,64,1"
- 17 Verify that VME light blinks, and that UUT board ID string is displayed: ()
- 18 Remove jumper from JB1-2 to JB1-11 on UUT
- 19 On the host console, enter "D 0xf07c0000,64,1"
- 20 Verify that VME light blinks, and that UUT board ID string is displayed: ()
- 21 Remove jumper from JB1-1 to JB1-12 on UUT
- 22 On the host console, enter "D 0xf0fc0000,64,1"
- 23 Verify that VME light blinks, and that UUT board ID string is displayed: ()

AUTOMATED TEST (V115)

- 1 Connect monitor to test card, and then press RESET button on Front End Host CPU.
- 2 Verify that message "(A)cceptance or (D)iagnosis test? (D)" appears on the operator terminal, ()
- 3 Press A key to run the acceptance test.
- 4 Follow the instructions that appear on the operator terminal for the rest of test.
- 5 Return to host console, at the prompt (=>) enter:

wfgFlash "/operations/rhicfec/release3.1/POWER3E/data/config/drivers/image.wfg", "/dev/wfg" for RHIC use or

wfgFlash "/operations/rhicfec/release3.1/POWER3E/data/config/drivers/wfgimageAGS", "/dev/wfg" for AGS use.

This loads the flash PROM with the operations code prior to field use. Press RESET button on UUT and verify that FAIL LED lights then goes out and then RUN LED is on. ()

- 6 Power off the test station and then remove UUT.
- 7 Re-install the jumpers on JB1 per the default jumper list. ()
- 8 Verify that NO ERRORS are reported on the printer's output, and sign here _____
- 9 File the hard copy of the test result along with this record.

AUTOMATED TEST (T115/T215)

- 1 Run V115 (D)iagnostic test with defaults of test 6 to test 19 with fibers connected to XMT_A and XMT_B of the T115/T215.
- 2 If a T215 is being tested repeat step 1 with fibers connected to XMT_2A and XMT_2B of the T215.
- 3 Press reset on the V115 and run (A)cceptance test for the T115.

V115 JUMPER SETTINGS

The V115 Board (WFG) has an address range from F000 0000 to F0FC 0000, A18 to A23 are jumper selectable. When the jumper is installed the bit is set to a zero, with the jumper out the bit is a one. As far as I know, based on the ATR line setup, the WFG boards are to be addressed as follows...

		A23	A22	A21	A20	A19	A18
1st WFG	F010 0000	X	X	X	---	X	X
2ndWFG	F014 0000	X	X	X	---	X	---
3rdWFG	F018 0000	X	X	X	---	---	X
4thWFG	F01C 0000	X	X	X	---	---	---
5thWFG	F020 0000	X	X	---	X	X	X
6thWFG	F024 0000	X	X	---	X	X	---
7thWFG	F028 0000	X	X	---	X	---	X
8thWFG	F02C 0000	X	X	---	X	---	---
9thWFG	F030 0000	X	X	---	---	X	X
10thWFG	F034 0000	X	X	---	---	X	---
11thWFG	F038 0000	X	X	---	---	---	X
12thWFG	F03C 0000	X	X	---	---	---	---
13thWFG	F040 0000	X	---	X	X	X	X
14thWFG	F044 0000	X	---	X	X	X	---
15thWFG	F048 0000	X	---	X	X	---	X
16thWFG	F04C 0000	X	---	X	X	---	---
17thWFG	F050 0000	X	---	X	---	X	X
18thWFG	F054 0000	X	---	X	---	X	---

and so on as needed. X indicates jumper installed (0), --- indicates jumper removed (1). Two other jumpers should always be installed, JP3 and JP4.

```
/* define test error code */

#define NO_ERROR          ( 0 )
#define MISMATCH         ( 1 )
#define NO_EVENT         ( 2 )
#define UNEXPECTED_EVENT ( 3 )
#define FIFO_FULL        ( 4 )
#define FIFO_EMPTY       ( 5 )
#define FIFO_NOT_FULL    ( 6 )
#define FIFO_NOT_EMPTY   ( 7 )
#define PARITY_ERROR     ( 8 )
#define FRAME_ERROR      ( 9 )
#define PHASE_ERROR      ( 10 )
#define CRC_ERROR        ( 11 )
#define NO_RDBACK        ( 12 )
#define UNEXPECTED_RDBACK ( 13 )
#define NO_720HZ_EVENT   ( 14 )
#define FAILED_TO_CLEAR_REG ( 15 )
#define FAILED           ( 0x10 )
#define UNEXPECTED_ERR   ( 0x11 )
#define UNEXPECTED_STATUS ( 0x12 )
```

RHIC POWER SUPPLY WAVEFORM GENERATOR PRINTS

94028108 MODULE ASSEMBLY
94028107 FRONT PANEL
94028106 PC BOARD ASSEMBLY
94028105 DRILL DRAWING
94028104 SCHEMATIC

PROGRAMMING THE ALTERA CHIPS

Select MAX+ icon from WINDOWS on the PC with the chip programmer attached. Click on MAX+plusII and select programmer. Double click on file name.

Set path to J:\RICPLD\9402\POF\ and select 8122.POF (LINK_INT.POF)for the programming file. Make sure the adapter PLMJ7000-84 is installed in the programmer and insert the EPM7128LC84-20 chip into the socket. Select program to burn the chip.

Checksum=00153B7A

Label chip-94028122

Select 8120.POF (MD_INT.POF) and program chip. (EPM7128LC84-20)

Checksum=001600A9

Label chip-94028120

Select 8121.POF and program chip. (EPM7160LC84-20) 2 chips are required to for each board.

Checksum=001C1DFA

Label chips-94028121

Install adapter PLMG7192 into programmer. Select 8124.POF and program chip. (EPM7192EGC160-20)

Checksum=002220EE

Label chip-94028124

Install adapter PLMJ7032 into programmer. Select 8123.POF and program chip. (EPM7032LC44-7)

Checksum=00063235

Label chip-94028123

Note: Chips were programmed using MAX PLUS version 5.1, when loading POF files a message that some files were not found may appear, click on OK, they are not necessary for programming.