

MADC SYSTEM TEST PROCEDURE

Note: This procedure tests the V113, V114, Buffered I/O panel, cable, and power supply.

File: `projects/test_procedures/v113_v114_test_pro.doc`

Equipment: Vme chassis
Fec (162-222)
Memory module (mm-6702)
Vmivme 4116, and test harness
Xterm
Calibrated voltage source
Calibrated function generator
Oscope
Dvm
Labview software
P2 jumper
Test V113
Test V114
Test made buffered i/o panel
Test made i/o cable
Test buffered made power supply

Setup:

1. install vme chassis
2. install FEC, 162-222, name acnfec119, in slot 1, connect network, connect xterm port1 to console1.
3. install memory module, mm-6702, slot 2.
4. install vmivme 4116, and test harness, slot 21.
5. install V113, address 540000, slot 11
6. install V114, slot 12.
7. install V113/V114 P2 jumper cable in back of chassis, slot 11/12.
8. install buffered made i/o panel, connect 4116 test harness,
 - J0 - brown - sine wave
 - J1 - short plug
 - J2 - red - sawtooth wave
 - J3 - short plug
 - J4 - orange - square wave
 - J5 - short plug
 - J6 - yellow - triangle wave
 - J7 - short plug
 - J8 - green - sine wave
 - J9 - short plug
 - J10 - blue - sawtooth wave
 - J11 - short plug
 - J12 - purple - square wave
 - J13 - short plug
 - J14 - grey - triangle wave
 - J15 - short plug
9. install made i/o cable, V114 chan 0-15 to i/o panel.
10. install made buffered i/o power supply.
11. turn on xterm and log in as a user.
12. open an xterm window, console window, and port1 window(alt-shift-pause)
13. turn on vme chassis and watch in port1 window as FEC boots.
14. when FEC has booted, in console window log into FEC:

```
telnet acnfec119
target
pass ord
```

15. in console window change directories:
cd"/home/cfsa/michnoff/madc/vx"
16. in console window initialize boards:
<init2
17. in terminal window set environment to acnec119:
setenv CD_HOST acnec119
18. in terminal window start labview:
labview
19. open all 5 labview windows:
ctl1.vi
ctl2.vi
graph1bw.vi
stat1.vi
stat2.vi
20. view stat1.vi while running ctl1.vi, should show:
V113 serial number
A32 address
A24 address
V114 voltage range
Stop ctl1.vi when done.
21. view stat2.vi while running and setting up ctl2.vi:
select scan group 1 and hit 'stop acq'
select scan group 0 and hit 'stop acq'
set up scan group 0:
scan group - 0
number of channels - 64
data format - 1
interrupt mode - on nth scan
int scan count - 1
buffer size - 3600
buffer top ptr - 512
arm setup - immediate on start
arm delay - 66000
halt setup - scan continuous
halt delay - 5000
scan setup - on clock (1cnt=1uS) no reset ctr
scan counter - 300
arm/halt trigger source - event
scan trigger source - event
a24 base address - 540000
hit 'load setup'
hit 'start acq'
22. view and setup graph1bw.vi
setup graph1bw.vi:
scan group - 0
full scale range - 20v
mode - bipolar
a24 address - 540000
start ptr - 0
using 'sequence' scan thru channels to verify input signals.
23. now that the complete madc test system is working you can replace any of the components and test a specific part.

V113 Testing

1. using previously setup mdc test system, power off vme chassis.
2. install TEST V113, check sysfail jumper, check for power shorts, set address to 540000
3. close labview, ctrl c.
4. power up test system, watch on port1 until FEC is booted, in console log into FEC:
telnet acnfec119
target
pass ord
5. load firmware in console window:
cd"/ride/firmware/mdc"
ld <MV162/mdcFlash
mdcFlash"I960/image",0xf0540000
relay should click and firmware should load.
6. verify firmware in console window:
d 0xf0540000,128,1
this will display ID prom and firmware date. As of Sept. 2001 this date is 2/16/99.
7. hit 'reset' on TEST V113, verify cpu runs with frontpanel LED's
8. test memory in console window:
cd"/home/cfsa/michnoff/mdc/vx"
<mdc_memtst1 (for 1Mb ram)
<mdc_memtst2 (for 2Mb ram)
verify no errors during memory tests.
9. initialize V113:
<init2
10. verify scan list memory in console window:
d 0xf0562000,256,1
11. verify event codes via console window:
list_ev 0 reads 01 48 back
list_ev 1 reads c0 back
list_ev 5 reads c0 back
12. verify scan group 0:
in the console window type--setenv CD_HOST acnfec119
open all 5 labview windows
run ctl2.vi, hit 'stop acq' for both scan group 0 and 1
set ctl2.vi to:
scan group - 0
number of channels - 64
data format - 1
interrupt mode - on nth scan
int scan count - 1
buffer size - 3600
buffer top prt - 512
arm setup - immediate on start
arm delay - 66000
halt setup - scan continuous
halt delay - 5000
scan setup - on clock (1cnt=1uS) no reset cntr
scan counter - 300
arm/halt trigger - event
scan trigger - event
a24 address - 540000
hit 'load setup' in ctl2.vi
hit 'start acq' in ctl2.vi
verify setup in stat2.vi
setup graph1bw.vi to:
sequence - yes

- chan - 0
 - elements - 1000
 - start ptr - 0
 - scan group - 0
 - full scale range - 20v
 - mode - bipolar
- run graph1bw.vi one channel at a time and verify:
 scan trigger out 0 LED is on
 signals on channels are the same as inputs
 scan trigger out 0 pulse. 500nS pulses every 300 uS or so.
13. verify external triggers
 - in ct12.vi window hit 'stop acq'
 - in ct12.vi set arm/halt trigger source to - extern 0
 - in ct12.vi set arm setup to - on trigger
 - hit 'load setup'
 - hit 'start acq'
 - in stat2.vi it should say waiting for arm trigger
 - connect a 1uS pulse every 1mS, +5v/gnd level, to external trigger 0 input, verify system triggered when cable was connected.
 - Repeat for triggers 1,2,3
 14. verify ADC error
 - in ct12.vi hit 'stop acq'
 - in ct12.vi set arm/halt trigger source to - event
 - in ct12.vi set arm setup to - immediate on start
 - in ct12.vi set scan counter to - 2
 - hit 'load setup'
 - hit 'start acq'
 - verify ADC error LED on V113 frontpanel comes on.
 15. verify eventlink
 - in ct11.vi hit 'run'
 - watch stat1.vi while plugging and unplugging the eventlink cable, verify eventlink LED, error on stat1.vi.
 - In ct11.vi hit 'stop'
 - In ct12.vi hit 'stop acq'
 - In ct12.vi set arm setup to - on trigger
 - In ct12.vi set eventcode to - co
 - In ct12.vi set scan counter back to - 300
 - In ct12.vi hit 'run'
 - Hit 'load setup'
 - Remove eventlink cable
 - Hit 'start acq'
 - View stat2.vi it should be waiting for arm trigger
 - Connect eventlink cable and verify it triggered
 16. verify scan group 1
 - in ct12.vi hit 'stop acq' for scan group 0 and 1
 - in ct12.vi setup scan group 0 to:
 - scan group - 1
 - number of channels - 1
 - data format - 1
 - int mode - on nth scan
 - int scan count - 1
 - buffer size - 3600
 - buffer top ptr - 524288
 - arm setup - immediate on start
 - arm delay - 66000
 - halt setup - scan continuously

halt delay - 5000
scan setup - on clock (1cnt=1uS) no reset cntr
scan counter - 300
arm/halt trigger source - event
scan trigger source - event
a24 address - 540000
hit 'load setup'
hit 'start acq'
in console type following command:
wrc 0xf0562080,0x82
in graph1bw.vi set to:
sequence - no
chan - 0
scan group - 1
in graph1bw.vi hit 'run'
verify in graph1bw.vi a sawtooth waveform, scan trigger 1 LED on frontpanel, and
500nS pulse every 300uS or so output.

17. verify simultaneous scan groups
in ct12.vi set up scan group 0 from step 12.
Hit 'load setup'
Hit 'start acq'
In graph1bw.vi view:
Scan group 1 chan 0 sawtooth waveform, LED and output pulse.
Scan group 0 all 64 channels, LED and output pulse.

18. verify remote reset
in console window type:
wrc 0xf056a009,0xab
wrc 0xf056a009,0x39
verify TEST V113 resets

19. Fill out V113 TEST sheet, file it, affix tested sticker, date and initials, database info.

V114 Testing

1. setup pcb jumpers for +-10V range
2. verify no shorts on pcb
3. plug in TEST V114 and measure +5,-5,+16,-16V are good
4. remove TEST V114 and add solder shorts to +16,-16,gnd, and start
5. reinstall TEST V114 and power up vme chassis
6. close old labview, cntrl-c.
7. open labview
 - open console window, terminal window, and port1 window
 - in console window log into FEC
 - telnet acnfec119
 - target
 - pass ord
 - in console change directories
 - cd"/home/cfsa/michnoff/madc/vx"
 - in console initialize setup
 - <init2
 - in terminal window set environment
 - setenv CD_HOST acnfec119
 - in terminal window start labview
 - labview
 - open the 5 labview windows
 - ctl1.vi
 - ctl2.vi
 - graph1bw.vi
 - stat1.vi
 - stat2.vi
8. calibrate common mode, CMRR
 - setup signal generator to output (50ohm) a perfect 20v p-p sinewave, +10v,-10v
 - connect signal generator and voltage source to TEST V114 chan 0-15 with the test cable
 - in console window set chan 0 to signal generator input
 - m 0xf0562080,0x82
 - 80
 - in ctl2.vi hit 'stop acq' for scan group 0 and 1
 - in ctl2.vi setup scan group 1 to
 - scan group - 1
 - number of channels - 1
 - data format - 1
 - buffer size - 3600
 - buffer top ptr - 524288
 - arm setup - immediate on start
 - arm delay - 66000
 - halt setup - scan continuous
 - halt delay - 50000
 - scan setup - on clock (1cnt=1uS) no reset cntr
 - scan counter - 300
 - arm/halt trigger source - event
 - scan trigger source - event
 - a24 address - 540000
 - hit 'load setup'
 - hit 'start acq'

```

in graph1bw.vi set to
  chan - 0
  scan group - 1
  number of elements - 1000
  start ptr - 0
  a24 address - 540000
  range - 20v
  mode - bipolar
in graph1bw.vi hit 'run'
calibrate CMRR pot until RMS noise is lowest, 1.5mV max
9. calibrate offset and gain
in console set chan 0 to input voltage source
  m 0xf0562080,0x82
  83
.
set input voltage source to 0V, calibrate offset pot to 0V (+-1.5mV)
set input voltage source to 9V, calibrate gain pot to 9V (+-1.5mV)
repeat until gain and offset are within specs
reverse polarity of input voltage source and check if its within specs
  at 0V and -9V
10. calibrate reference voltages
in ctl1.vi hit 'run'
in ctl1.vi set to 'ref voltages'
in ctl1.vi click on white box to set ref voltages
in console window set chan 0 to chan 62 (+5V)
  m 0xf0562080,0x82
  bf
.
in grap1bw.vi, calibrate ref pots until +5 is within specs (+-1.5mV)
in console window set chan 0 to chan 63 (-5V)
  m 0xf0562080,0x82
  be
.
view graph1bw.vi to check -5V is within specs (+-1.5mV)
11. check settling time
in ctl2.vi hit 'stop acq' for both scan group 0 and 1
set ctl2.vi to
  scan group - 1
  number of channels - 1
  data format - 1
  interupt mode - none
  int scan count - 1
  buffer size - 3600
  buffer top ptr - 524288
  arm setup - immediate on start
  arm delay - 66000
  halt setup - halt when buffer full
  halt delay - 50000
  scan setup - on clock (1cnt=1uS) no reset cntr
  scan counter - 0
  arm/halt trigger source - event
  scan trigger source - event
  a24 address - 540000
hit 'load setup'

```

in console window set chan 0 to +5V reference
m 0xf0562080,0x82
bf

.
in ctl2.vi hit 'start acq' to take a snap shot of the +5V
in graph1bw.vi hit run once to view data, +5V
in console set chan 0 to -5V reference
m 0xf0562080,0x82
be

.
in ctl2.vi hit 'start acq' to take a snap shot of the -5V
in graph1bw.vi hit 'run' once to view that data, -5V.
use the magnify function to view how long it takes to go from +5v to -5v,
the settling time, should be not more than 2 counts or 2uS.

In ctl2.vi hit 'stop acq'
In ctl2.vi set
Scan counter - 2
Hit 'load setup'
Hit 'start acq'
View the -5v data in graph1bw.vi
In console set chan 0 to 0V, set input voltage source to 0V
M 0xf0562080,0x82
83

.
in ctl2.vi hit 'start acq'
in graph1bw.vi hit 'run'
view data, record 0V average/rms noise values for 2uS
in ctl2.vi hit 'stop acq'
in ctl2.vi change scan counter to - 4
hit 'load setup'
in console set chan 0 to -5v
m 0xf0562080,0x82
be

.
in ctl2.vi hit 'start acq'
in graph1bw.vi hit 'run'
view -5v data
in console set chan 0 to 0V, set input voltage source to 0V
m 0xf0562080,0x82
83

.
in ctl2.vi hit 'start acq'
in graph1bw.vi hit 'run'
view data, record 0V average/rms noise values for 4uS

12. check a/d voltage range

in ctl1.vi hit 'run'
view voltage range in stat1.vi, should be -10 to +10

13. check 0V average/noise

in ctl2.vi set
halt setup - scan continuous
scan counter - 300
hit 'load setup'
hit 'start acq'
view 0V data in graph1bw.vi

record data

14. test all inputs with grounds/waveforms
 - hit 'stop acq' for scan group 0 and 1
 - in ct11.vi turn off reference voltages, turn on chan 62/63
 - setup ct12.vi as follows
 - scan group - 0
 - number of channels - 64
 - data format - 1
 - interrupt mode - on nth scan
 - int scan count - 1
 - buffer size - 3600
 - buffer top ptr - 512
 - arm setup - immediate on start
 - arm delay - 66000
 - halt setup - scan continuous
 - halt delay - 5000
 - scan setup - on clock (1cnt=1uS) no reset ctr
 - scan counter - 300
 - arm/halt trigger source - event
 - scan trigger source - event
 - a24 base address - 540000
 - hit 'load setup' for scan group 0
 - hit 'start acq' for scan group 0
 - setup input signals as follows
 - J0 - brown - sine wave
 - J1 - short plug
 - J2 - red - sawtooth wave
 - J3 - short plug
 - J4 - orange - square wave
 - J5 - short plug
 - J6 - yellow - triangle wave
 - J7 - short plug
 - J8 - green - sine wave
 - J9 - short plug
 - J10 - blue - sawtooth wave
 - J11 - short plug
 - J12 - purple - square wave
 - J13 - short plug
 - J14 - grey - triangle wave
 - J15 - short plug
 - Connect i/o cable to TEST V114 chan 0-15
 - In graph1bw.vi view scan group 0 all channels, reconnect made i/o cable
To chan 16-31, 32-47, 48-63.
 - Next swap grounds for signals on the j inputs and retest all channels.
15. fill out V114 test sheet, affix test sticker, date and initials, database info.

MADC I/O PANEL or CABLE TESTING

1. install i/o panel or cable into test setup
2. using graph1bw.vi test all channels with grounds and signals
3. record test sheet for i/o panel results, place a tested sticker on unit with initials and date, database info
4. i/o cables place a tested sticker with initials and date

MADC BUFFERED I/O POWER SUPPLY

1. connect a 7.5 ohm test load connector to the output, along with a volt meter
2. plug in the 110vac input and verify the output is on and at least +-10.5VDC
3. place a tested sticker on the unit with initials and a date, database info.

MADC V113 CONTROLLER BOARD TEST REPORT

SERIAL NO.: _____

DATE: _____

ENGINEER/TECHNICIAN: _____

1. CHECK +5V TO GND CONTINUITY _____
2. VERIFY SYSFAIL JUMPER _____
3. VERIFY A24 AND A32 ADDRESS SWITCH SELECTION _____
4. VERIFY FLASH MEMORY PROGRAMMING _____
5. VERIFY ID. PROM _____
6. VERIFY THE i960 CPU PROGRAM RUNS AND THE FRONT PANEL LEDS ILLUMINATE WITH
RESET _____
7. VERIFY MEMORY TESTS _____
8. VERIFY SCAN LIST MEMORY _____
9. VERIFY EVENT CODES _____
10. VERIFY SCAN GROUP 0 DATA ACQUISITION

SCAN TRIG OUT 0 INDICATOR _____
CH. 0 SINE WAVEFORM _____
SCAN TRIG OUT 0 OUTPUT _____
11. VERIFY EXTERNAL TRIGGER INPUTS _____
12. VERIFY ADC ERR INDICATOR _____
13. VERIFY EVENT LINK _____
14. VERIFY SCAN GROUP 1 DATA ACQUISITION

SCAN TRIG OUT 1 INDICATOR _____
CH. 0 SAWTOOTH WAVEFORM _____
SCAN TRIG OUT 1 OUTPUT _____
15. VERIFY SIMULTANEOUS SCAN GROUP _____
16. VERIFY REMOTE RESET _____

RHIC MADC V114 Multiplexed Analog to Digital Converter Module Test Report

Serial Number: _____ Date: _____

Engineer/Technician: _____

-10V to +10V Range Tests

Settles to ± 1 count in 2 μ s from -9.7V to 0V: _____

A/D board Voltage Range status: _____

Chan 62 Ref Average: _____ RMS Noise: _____

Chan 63 Ref Average: _____ RMS Noise: _____

Chan 23 0V Average: _____ RMS Noise: _____

Chan 5 0V (scanned after square wave)

(2 μ s settling time) Average: _____ RMS Noise: _____

(4 μ s settling time) Average: _____ RMS Noise: _____

Data as expected with even channel cable (chans 0 to 63): _____

Data as expected with odd channel cable (chans 0 to 63): _____

-5V to +5V Range Tests

A/D board Voltage Range status: _____

Chan 62 Ref Average: _____ RMS Noise: _____

Chan 63 Ref Average: _____ RMS Noise: _____

Chan 23 0V Average: _____ RMS Noise: _____

Chan 5 0V (scanned after square wave)

(2 μ s settling time) Average: _____ RMS Noise: _____

(4 μ s settling time) Average: _____ RMS Noise: _____

Data as expected with even channel cable (chans 0 to 15): _____

0V to +10V Range Tests

A/D board Voltage Range status: _____

Chan 62 Ref Average: _____ RMS Noise: _____

Chan 63 Ref Average: _____ RMS Noise: _____

Chan 23 0V Average: _____ RMS Noise: _____

Chan 5 0V (scanned after square wave)

(2 μ s settling time) Average: _____ RMS Noise: _____

(4 μ s settling time) Average: _____ RMS Noise: _____

Data as expected with even channel cable (chans 0 to 15): _____