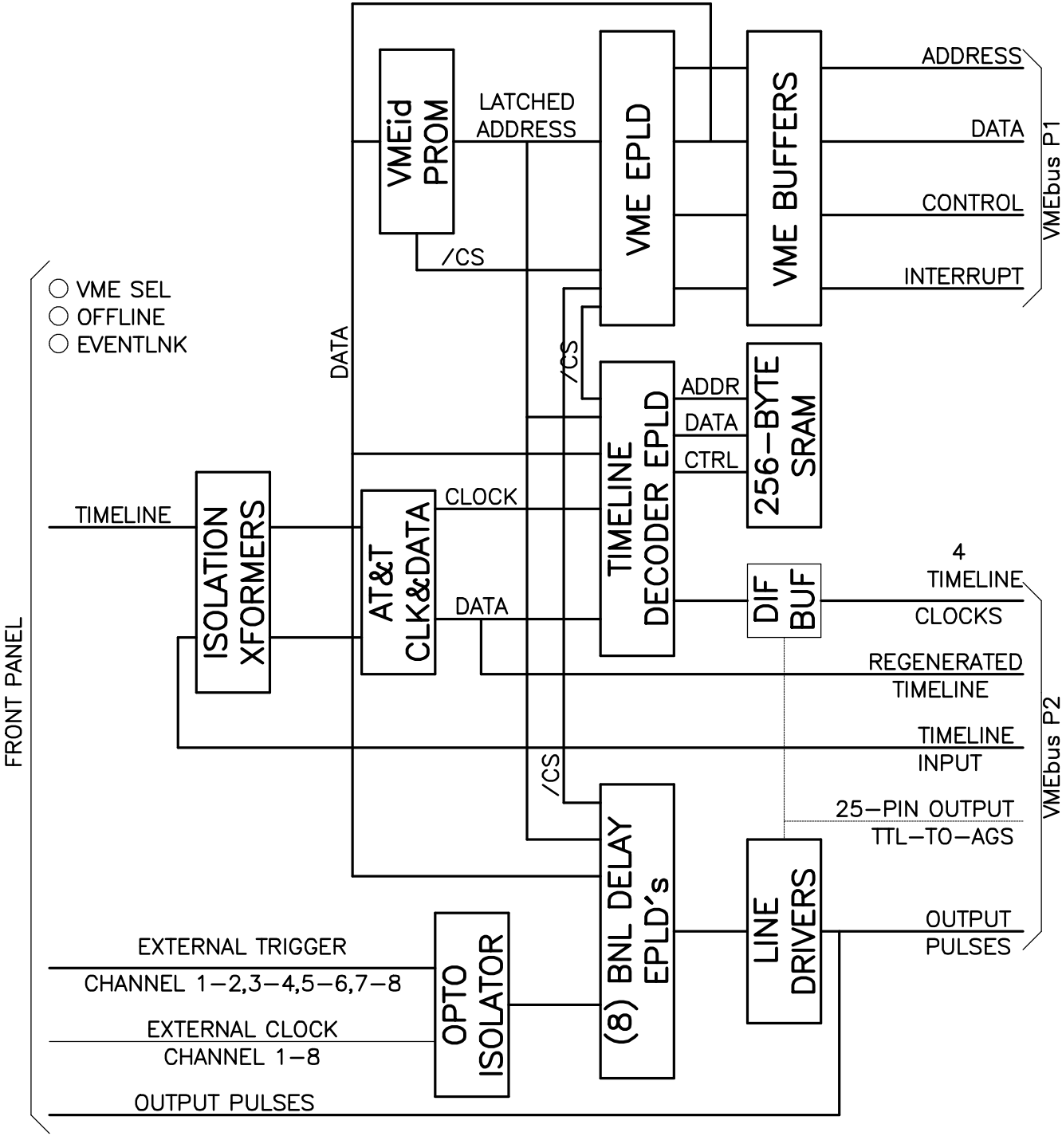
FRONT PANEL
VME SEL
OFFLINE
EVENTLNK
TIMELINE
ISOLATION XFORMERS
DATA
VMEid PROM
/CS
LATCHED ADDRESS
VME EPLD
VME BUFFERS
ADDRESS
DATA
CONTROL
INTERRUPT
VMEbus P1
/CS
TIMELINE DECODER EPLD
ADDR
DATA
CTRL
256-BYTE SRAM
AT&T CLK&DATA
CLOCK
DATA
DIF BUF
4 TIMELINE CLOCKS
REGENERATED TIMELINE
TIMELINE INPUT
VMEbus P2
/CS
(8) BNL DELAY EPLD's
25-PIN OUTPUT TTL-TO-AGS
LINE DRIVERS
OUTPUT PULSES
EXTERNAL TRIGGER
CHANNEL 1-2,3-4,5-6,7-8
EXTERNAL CLOCK
CHANNEL 1-8
OPTO ISOLATOR
OUTPUT PULSES