RHIC
1024Frev DDS

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REV. 3

OVERVIEW

The 1024Frev Direct Digital Synthesizer (DDS) is a low noise clock that serves as the master clock for all of the low level Direct Digital Synthesizers in the system. A second DDS serves as the Radial Steering L.O.. Real time frequency data is sent from the DSP via a communications port at Frev (78KHz). The intermediate frequency (IF) used for the Radial LO down conversion, and the Harmonic Number are programmable via an on board VME interface. All VME address and data modes are supported. The present programmable configuration is to support the A32 extended mode.

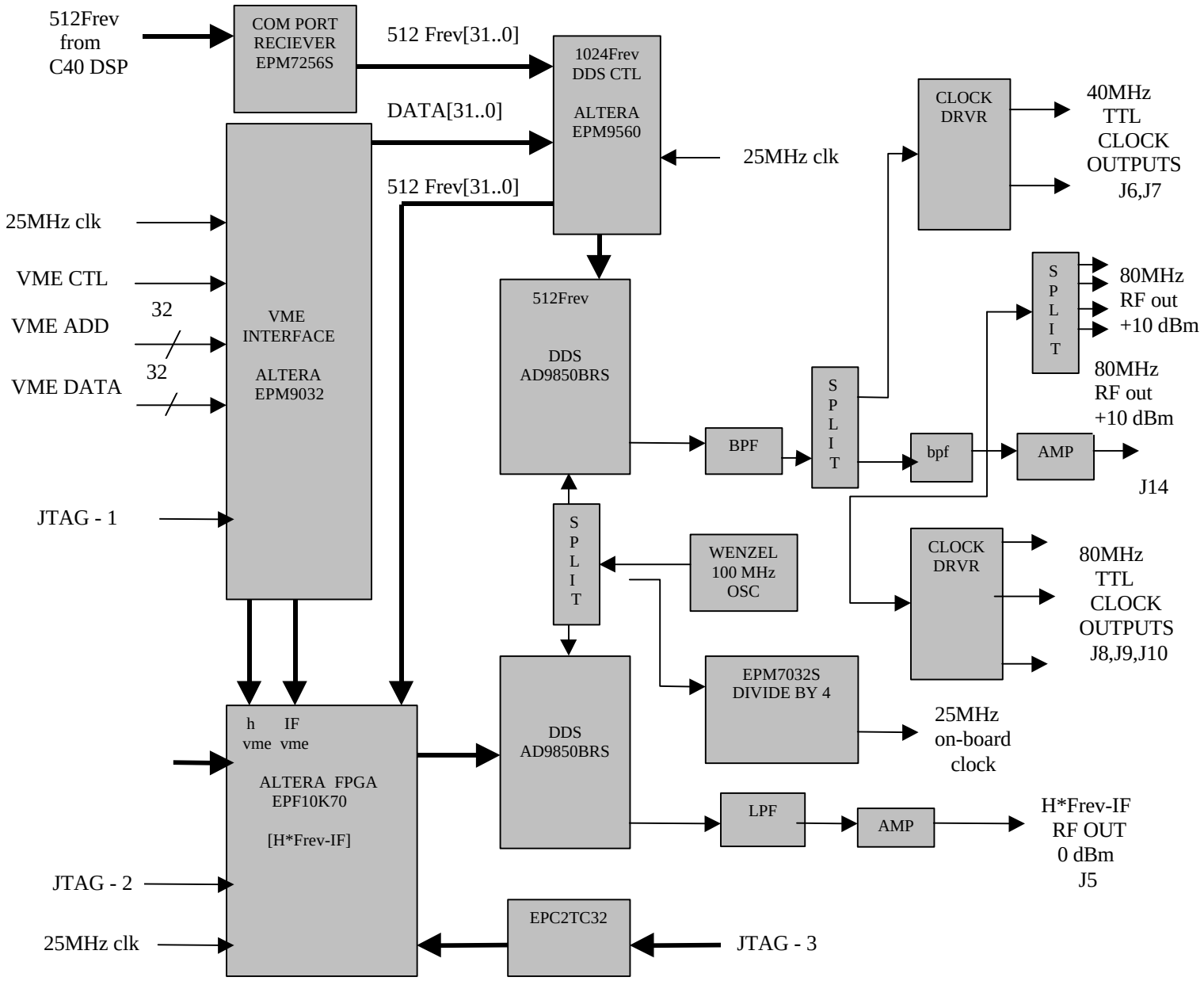
Output frequencies are derived from a low noise 100 MHz Wenzel crystal oscillator. The oscillator is split to feed two on board Analog Devices 9850BRS DDS synthesizers. The output of the first DDS is 40 MHz (nominal). This 40 MHz is split with one leg feeding a frequency doubler. The doubler output is also split with one leg feeding an RF amplifier to provide an 80 MHz +10dBm RF output, and the other leg feeds a digital clock driver to provide multiple 80 MHz TTL clock outputs.

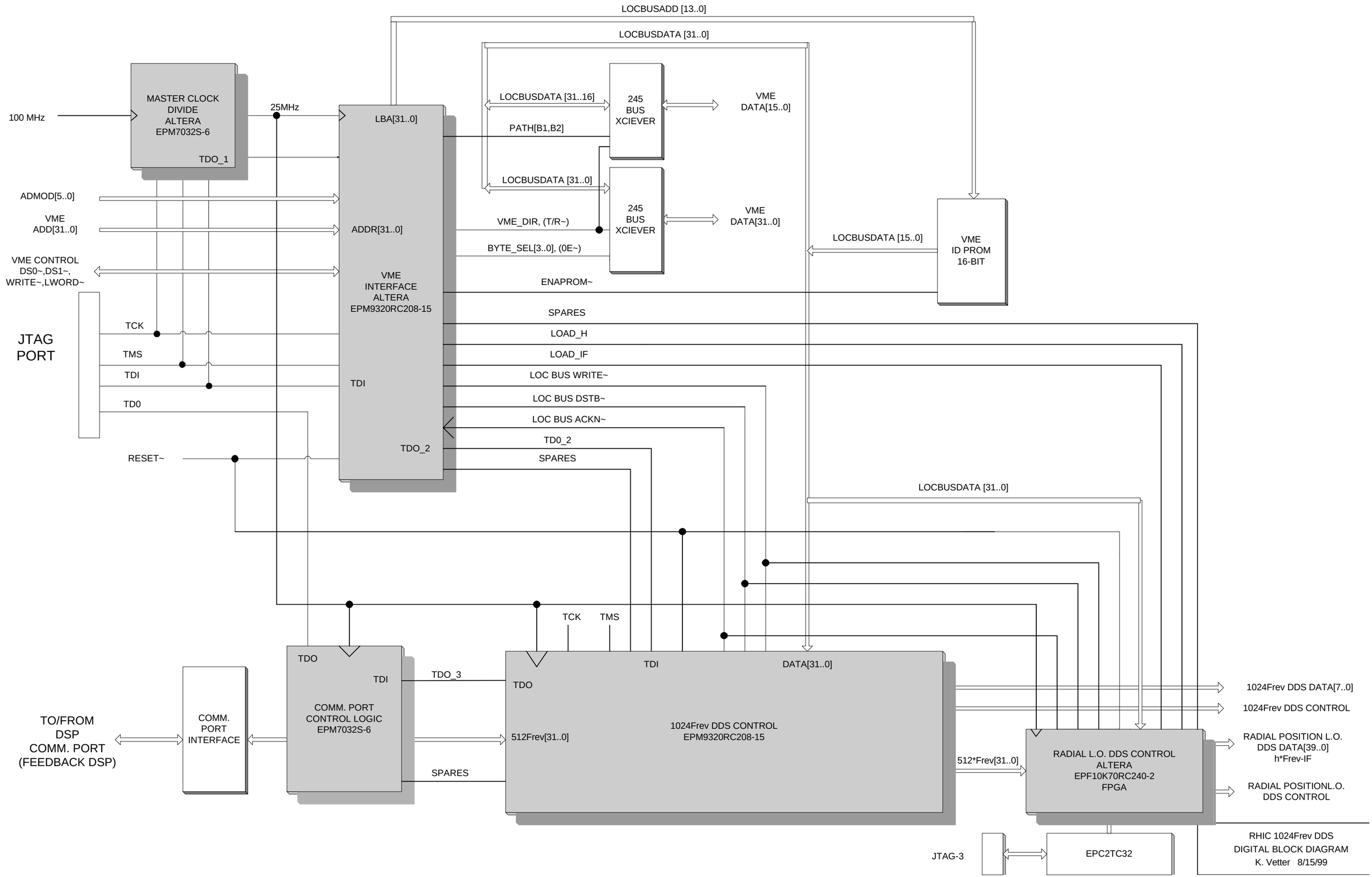
The harmonic number (h) and intermediate frequency (IF) are read in as digital words over the VME data bus. An on board Field Programmable Gate Array (Altera EPF10K70) calculates [h*Frev-IF] which is the frequency word for the Radial Steering L.O. DDS. For h=480, and IF=10.7MHz the Radial Steering output is 26.74 MHz. This is well within the Nyquist frequency of 50MHz so that a reasonable anti-aliasing filter is realizable. The output of this synthesizer is bandpass filtered and amplified to +10dBm.

TABLE 1 (SPECIFICATIONS)

PARAMATER	DESCRIPTION	SPECIFICATION	COMMENT
PHASE NOISE	dBc/Hz	-132 @ 100 Hz	80MHz RF output
	dBc/Hz	-157 @ 1 KHz	80MHz RF output
	dBc/Hz	-167 @ 10 KHz	80MHz RF output
	dBc/Hz	-171 @ 20 KHz	80MHz RF output
	dBc/Hz	-130 @ 100 Hz	[h*Frev-IF] output
	dBc/Hz	-155 @ 1 KHz	[h*Frev-IF] output
	dBc/Hz	-165 @ 10 KHz	[h*Frev-IF] output
	dBc/Hz	-169 @ 20 KHz	[h*Frev-IF] output
Frequency Resolution	DDS frequency resolution	9.3 mHz @ 80 MHz	32 bit frequency tunning
Phase Resolution	DDS phase resolution	11.25 deg.	5 bit phase tunning
Output Power	1024Frev RF output	+10 dBm	J14
Output Power	1024Frev RF output	0 dBm	J11, J12, J13
Output Power	Radial Position L.O.	+10 dBm	J5 [h*Frev-IF] output
80 MHz Clock output	1024Frev digital output	TTL	J8, J9, J10
40 MHz Clock output	512Frev digital output	TTL	J6, J7
Communication Port	4-byte transfer per request	TTL	TMS320C40 interface
Image Rejection	DDS Image	> 60 dB	80 MHz RF output
Image Rejection	DDS Image	> 60 dB	[h*Frev-F] output
VME address space	Board base address range	A32 Extended	0x00040000–0x00050000
Harmonic number	Write Harmonic Number	A32 Extended	0x00040000
IF Frequency	Write Intermidiate Freq.	A32 Extended	0x00040001

BLOCK DIAGRAM (1024Frev DDS)




LOCBUSADD [13..0]
LOCBUSDATA [31..0]
MASTER CLOCK
DIVIDE
ALTERA
EPM7032S-6
TDO_1
100 MHz
25MHz
LBA[31..0]
LOCBUSDATA [31..16]
245
BUS
XCIEVER
VME
DATA[15..0]
PATH[B1,B2]
LOCBUSDATA [31..0]
245
BUS
XCIEVER
VME
DATA[31..0]
ADMOD[5..0]
VME
ADD[31..0]
ADDR[31..0]
VME_DIR, (T/R~)
BYTE_SEL[3..0], (0E~)
LOCBUSDATA [15..0]
VME
ID PROM
16-BIT
VME CONTROL
DS0~,DS1~,
WRITE~,LWORD~
VME
INTERFACE
ALTERA
EPM9320RC208-15
ENAPROM~
SPARES
JTAG
PORT
TCK
TMS
TDI
TD0
LOAD_H
LOAD_IF
TDI
LOC BUS WRITE~
LOC BUS DSTB~
LOC BUS ACKN~
TD0_2
TDO_2
SPARES
RESET~
LOCBUSDATA [31..0]
TCK
TMS
TDO
TDI
TDO_3
TDO
TDI
DATA[31..0]
TO/FROM
DSP
COMM. PORT
(FEEDBACK DSP)
COMM.
PORT
INTERFACE
COMM. PORT
CONTROL LOGIC
EPM7032S-6
512Frev[31..0]
1024Frev DDS CONTROL
EPM9320RC208-15
SPARES
1024Frev DDS DATA[7..0]
1024Frev DDS CONTROL
RADIAL POSITION L.O.
DDS DATA[39..0]
h*Frev-IF
512*Frev[31..0]
RADIAL L.O. DDS CONTROL
ALTERA
EPF10K70RC240-2
FPGA
RADIAL POSITIONL.O.
DDS CONTROL
JTAG-3
EPC2TC32
RHIC 1024Frev DDS
DIGITAL BLOCK DIAGRAM
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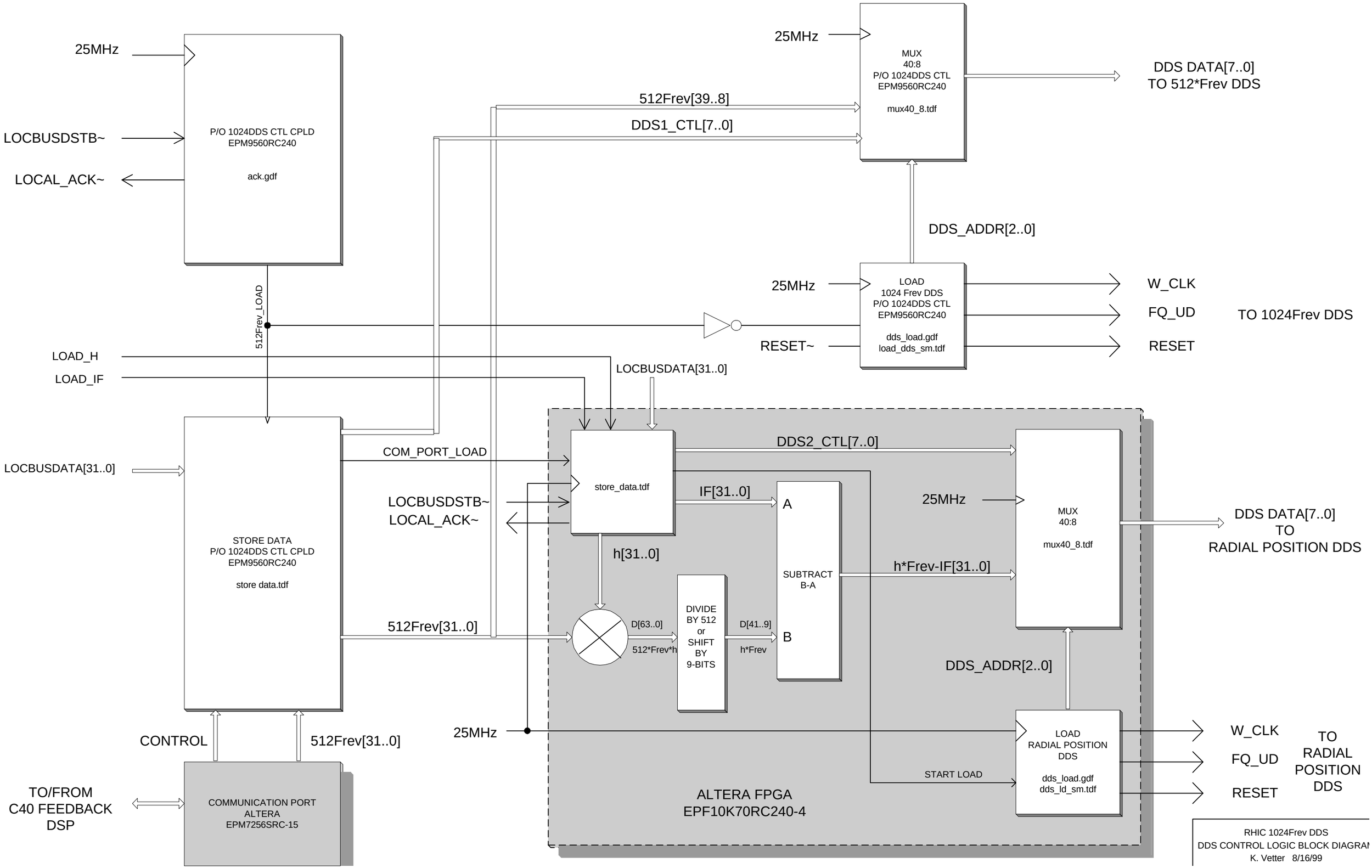
25MHz
P/O 1024DDS CTL CPLD
EPM9560RC240
ack.gdf
LOCBUSDSTB~
LOCAL_ACK~
25MHz
MUX
40:8
P/O 1024DDS CTL
EPM9560RC240
mux40_8.tdf
DDS DATA[7..0]
TO 512*Frev DDS
512Frev[39..8]
DDS1_CTL[7..0]
DDS_ADDR[2..0]
25MHz
LOAD
1024 Frev DDS
P/O 1024DDS CTL
EPM9560RC240
dds_load.gdf
load_dds_sm.tdf
RESET~
W_CLK
FQ_UD
RESET
TO 1024Frev DDS
512Frev_LOAD
LOAD_H
LOAD_IF
LOCBUSDATA[31..0]
LOCBUSDATA[31..0]
STORE DATA
P/O 1024DDS CTL CPLD
EPM9560RC240
store data.tdf
COM_PORT_LOAD
LOCBUSDSTB~
LOCAL_ACK~
512Frev[31..0]
store_data.tdf
DDS2_CTL[7..0]
IF[31..0]
h[31..0]
A
SUBTRACT
B-A
B
25MHz
MUX
40:8
mux40_8.tdf
DDS DATA[7..0]
TO
RADIAL POSITION DDS
h*Frev-IF[31..0]
D[63..0]
512*Frev*h
DIVIDE
BY 512
or
SHIFT
BY
9-BITS
D[41..9]
h*Frev
DDS_ADDR[2..0]
25MHz
CONTROL
512Frev[31..0]
LOAD
RADIAL POSITION
DDS
dds_load.gdf
dds_ld_sm.tdf
START LOAD
W_CLK
FQ_UD
RESET
TO
RADIAL
POSITION
DDS
TO/FROM
C40 FEEDBACK
DSP
COMMUNICATION PORT
ALTERA
EPM7256SRC-15
ALTERA FPGA
EPF10K70RC240-4
RHIC 1024Frev DDS
DDS CONTROL LOGIC BLOCK DIAGRAM
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1024Frev DDS OUTPUT FREQUENCY and 28MHz
DDS OUPUT FREQUENCY CALCULATIONS
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$Fclk := 100$ MHz 512Frev DDS clock frequency

$DDS_freq := 10, 11 .. 42$ MHz 512Frev DDS output frequency

$freq_word_{DDS_freq} := \left(\frac{DDS_freq}{Fclk}\right) \cdot 2^{32}$ frequency word for the 512Frev DDS

DDS frequency word in hex.

$freq_word_{DDS_freq} =$

	0
0	429496729.6
1	472446402.56
2	515396075.52
3	558345748.48
4	601295421.44
5	644245094.4
6	687194767.36
7	730144440.32
8	773094113.28
9	816043786.24
10	858993459.2
11	901943132.16
12	944892805.12
13	987842478.08
14	$1.03079215 \cdot 10^9$
15	$1.07374182 \cdot 10^9$
16	$1.1166915 \cdot 10^9$
17	$1.15964117 \cdot 10^9$
18	$1.20259084 \cdot 10^9$
19	$1.24554052 \cdot 10^9$
20	$1.28849019 \cdot 10^9$

output frequency of 512Frev DDS before frequency doubler

$DDS_freq =$

10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30

MHz

1024Frev DDS output frequency calculations based on Cavity Tunning Range
Cavity frequency ranges from 28.15 MHz (high end) down approximatly 1% (281.5 KHz) or 27.8685 MHz.

$DDS_freq := 28 \cdot 10^6$

$Fclk := 80 \cdot 10^6$

$freq_word := \frac{DDS_freq}{Fclk} \cdot 2^{32}$ $\quad$ $freq_word = 59999999.99ah$

$DDS_freq_upper := 28.15 \cdot 10^6$ $\quad$ Upper limit of cavity frequency

$Fclk_upper := \left(\frac{DDS_freq_upper}{freq_word}\right) \cdot 2^{32}$ $\quad$ $Fclk_upper = 8.043 \cdot 10^7$ Hz

$DDS_freq_lower := 27.8685 \cdot 10^6$ $\quad$ lower limit of cavity frequency

$Fclk_lower := \left(\frac{DDS_freq_lower}{freq_word}\right) \cdot 2^{32}$ $\quad$ $Fclk_lower = 7.962 \cdot 10^7$ Hz

DDS SYSTEM FREQUENCY CALCULATIONS

$$fw1 := \frac{40 \cdot 10^6}{100 \cdot 10^6} \cdot 2^{32}$$

Frequency word for 512Frev DDS, from COM. PORT

$$fw2 := \frac{28 \cdot 10^6}{80 \cdot 10^6} \cdot 2^{32}$$

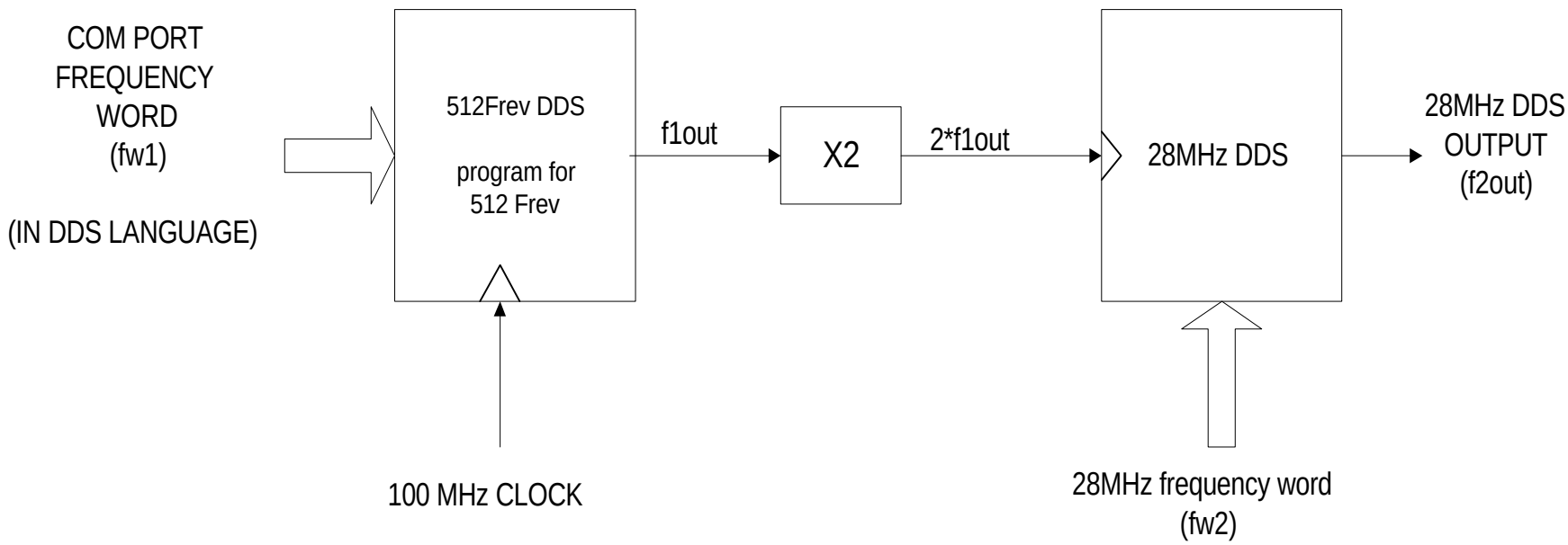
$fw2 = 1.503 \cdot 10^9$ $\quad$ $fw2 = 59999999.99ah$

$$f1out := \frac{fw1}{2^{32}} \cdot 100 \cdot 10^6$$

1024Frev output frequency

$$f2out := \frac{fw2}{2^{32}} \cdot 2 \cdot f1out$$

28MHz output frequency



$$f2out := 2 \cdot \frac{fw2 \cdot fw1}{2^{64}} \cdot 100 \cdot 10^6$$

output frequency of 28MHz DDS (Hz)

$f2out = 2.8 \cdot 10^7$ Hz

Radial Frequency Calculation

5/27/99

$h := 480$

$fclk := 100 \cdot 10^6$

$fout := 40 \cdot 10^6$ DDS output frequency, Hz

$IF_freq := 10.7 \cdot 10^6$

$frev := 78000$

$freq_word := \left(\frac{fout}{fclk}\right) \cdot 2^{32}$ $freq_word = 1.71798692 \cdot 10^9$ Hz $freq_word = 66666666.6666h$

$DDS_freq := \left(\frac{freq_word}{2^{32}}\right) \cdot fclk$ $DDS_freq = 4 \cdot 10^7$ Hz

$F_RLO := \frac{h \cdot freq_word}{512} - \left(\frac{IF_freq}{fclk}\right) \cdot 2^{32}$

$F_RLO = 449ba5e3.53fh$

Check Radial LO frequency tunning word

$F_rlo := 26.8 \cdot 10^6$

$Radial_LO_freq_word := \left(\frac{F_rlo}{fclk}\right) \cdot 2^{32}$ $Radial_LO_freq_word = 449ba5e3.53f8h$

$Radial_LO_freq_word = 1.15105124 \cdot 10^9$

$if_DDS_word := \frac{IF_freq}{fclk} \cdot 2^{32}$ $if_DDS_word = 459561500.672$