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DESIGN AND TEST OF A PHASE SHIFTER UTILIZING A PHASE LOCK LOOP (PLL)

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INTRODUCTION

The purpose of this research was to phase shift a 26.7 MHz sinusoidal voltage with an analog control voltage . This paper covers work done with a phase shifter implemented by a Phase Locked Loop (PLL). The purpose was achieved to the extent that the waveform was phase locked and phase shift was done over a limited range less than 180°.

CONTENT

In order to phase shift a sinusoid of frequency f1 using a PLL, it was necessary to create the circuit shown in Figure 1. The control voltage (Vadj) adjusts the phase by changing the frequency of the VCO. But before the circuit can phase shift, it must first be locked in frequency (i.e., when f1=f2). In order for lock to occur, the summer and active loop filter must be designed to meet the requirements of the Phase Detector (PD) and the Voltage Controlled Oscillator (VCO). Since the PD & VCO were pieces of equipment found in the lab that were not specifically designed for use in a PLL, the characteristics of these pieces had to be determined. More specifically, the input and output power (& voltage) requirements of the VCO & PD, as well as the output voltage-to-phase relationship of the PD and the input voltage-to-FM relationship of the VCO, were considered.

The voltage-to-phase relationship of the PD is shown in Fig. 2. From the data points it can be seen that in the first quadrant the plot is linear from about 19° to125° within

positive slope. The PLL is not expected to phase shift much more beyond this range since the PLL loses lock once the PD output becomes highly nonlinear. The slope of this line is 8.04 mv/° (=Kd). Now, the VCO FM relationship was found to be programmable, so the maximum setting was used (Ko=100 kHz/volt). The maximum setting was used since it was shown that the higher the FM setting, the smaller the phase jitter. The RF input power into the PD from the Stanford Research Systems (SRS) frequency generator was set to 11.21 dBm, whereas the output IF voltage of the PD was found to be 2.67v pp. However, the max input to the VCO was +/- 1v. It's output power was set to +10dBm. Using this data, the voltage summer and adjustable circuits were made as shown in Figure 3. The adjustable voltage had a range of +/- 280mv.

Originally, the active loop filter used was just a Bead-Pull integrator circuit found in the lab (see Figure 4). However, using this circuit prevented the PLL from locking. (Note: the method used to determine if the PLL was locked was to take f1 (as channel 3 input on the scope) and to trigger the scope with it. Using f2 as channel 4 input, it could be determined if the PLL was locked by just seeing when f2 was triggered and became the same frequency as f1, although not necessarily the same phase as f1.

In fact, the PLL locked, as evidenced by the error voltage remaining after the integrator was driven to an average of zero, but a large amout of phase jitter remained. This was due to the output of the Bead Pull integrator which had an unwanted AC voltage component on the error voltage with a value of 40mv pp (Max) and a frequency that shifted anywhere from 588 Hz to 1.7 kHz, depending upon the adjustable voltage applied. The AC component acted to phase modulate f2. As a result, a new active loop filter was designed

with a lower cutoff frequency.[3,4] The resulting circuit is shown in Figure 5. There were several major changes made in this circuit that made it differ from the Bead Pull circuit. One change made was that capacitors (2 pF & 10 pF) were added across each op amp, from the output to the input, as well as 220 Ω resistors added to the output of each op amp. These two changes were made to eliminate feedback that would cause unwanted oscillations. Another change made was that 2 kΩ resistors were added to each input of each op amp to reduce the input bias currents. This change reduces the error caused by drifts in offset currents due to temperature changes. A more significant change made was that two cutoff frequencies (100 Hz & 800 Hz) were introduced, both of them being much lower than the Bead Pull's cutoff freq. These changes were based on:

$1/R2C = 1/100Hz$ $\quad$ $C=4.7\mu F$ $\quad$ $R2=1.3k\Omega$

$1/((R1/2)C3) = 1/800Hz$ $\quad$ $C3=0.022\mu F$ $\quad$ $R1/2=10\ k\Omega$

Making the cutoff frequencies for the active loop filter this low would eliminate the 588 Hz- 1.7kHz phase jitter. Lastly, a change was made by adding a resistor in series with the 4.7μF feedback capacitor across the op amp.This not only slowed the integrator down, but also created a low pass (LP) filter. As shown on

page 39 of the *Phase Locked Loop Circuit Design* book, using this filter reduces the phase jitter and suppresses the high frequency components by introducing an additional pole. The resulting circuit is shown in Figure 6. The attenuators are used to reduce noise and to make the power levels of both signal generators the same. The LP filter used takes out the 53 MHz (2 x 26.7MHz) component from the PD.

The PLL locked, but only with the addition of a small voltage. Phase shift was possible by adjusting the voltage only a few millivolts, positive or negative, around zero. The maximum range of phase shift was about 160°. This covers the range of the linear region of the PD & a little beyond that (see Fig. 2 and Fig. 7 for a comparison; Fig. 7a shows the maximum absolute phase difference attained, with Fig. 7b showing the maximum amplitude deviations, while Fig. 7c shows a more conservative measurement). The tolerance of the phase is about +/- 4°, whereas the magnitude of the waveform is very stable, mainly due to the high accuracy of the HP VCO. Looking at the frequency response in Fig. 8, it can be seen that the two cutoff frequencies are at about 200 Hz and 1.1 kHz. This is slightly higher than the calculated 100 Hz & 800 Hz. Also, there seems to be higher order terms that cause the filter to pass some higher frequency components. Looking at Fig. 9, the curve fit poles and zeros seem to corroborate this fact. (Note: The frequency response curves were obtained using the 3562A HP Dynamic Signal Analyzer in the setup shown in Fig. 10, whereas the phase & magnitude

measurement curves were obtained using the HP 8573C Network Analyzer, in the setup shown in Fig. 11.)

It should be mentioned that when adding the voltage to get the PLL into lock, the voltage adjustment must be a slow transition, or else the PLL does not even lock. Once possibility for this happening is that when the cutoff frequencies were made too low, it reduced the bandwidth of the PLL by so much, that rapid changes in voltage were sacrificed, since once you are outside the bandwidth, you lose lock. So, there may be a compromise between the phase jitter and the bandwidth. In fact, the VCO must have at least $\omega 2 = \omega 1 +- d\theta 2/dt$ for a frequency range. Since Vadj modulates $\Delta\omega 2$ while modulating $\theta 2$ (& since $\Delta\omega 2 = d\theta 2/dt$ & since $\omega 2 = \omega 1 + \Delta d\theta o/dt$). $\theta 2(t) = (1/Kd)$ Vadj if PLL has $K >= 2$ Bm, where Bm = PLL bandwidth.[3]

Another thing which should be mentioned is that the critical value of DC voltage driving the VCO required for lock is:

(Pull-in voltage) $Vp = Kd\ [\ \Delta\omega/K - \sqrt{(\Delta\omega/K)^2 - 1}]$

where $K = KdKoKh$ (Kh = gain of active filter)

$\Delta\omega = \omega 2 - \omega 1$

The only problem is that experimentally it is difficult to measure some of these parameters.[3]

CONCLUSION

The intended goal to phase shift a sinusoid with an analog voltage using a phase

locked loop was achieved to the extent that phase shift was done over a range less than 180° and with a tolerance of +/- 4°. However, the PLL as a whole was extremely sensitive to changes in the control voltage. only a few millivolts, or were needed to change the phase in a dramatic way. Any attempts to place the entire PLL circuit into a small project box should consider this applied voltage. Any phase jitter due to low (& high) frequency components should by attenuated as much as possible using low pass filters. It may be possible to reduce some of the phase tolerance by limiting the cable lengths. Also, when constructing such a compact PLL, a high accuracy VCO should be considered as well.

ACKNOWLEDGEMENTS

The authors would like to thank Emmanuel Onillon for providing his assistance in using the 3562A HP Dynamic Signal Analyzer.

REFERENCES

1 - *Electrical Engineering Concepts & Applications* by Carlson & Gisser, c 1990

2 - *Analog Electronics Circuits: Analysis & Applications* by Robert Northrop, c 1990

3 - *Phase Locked Loop Circuit Design* by Dan H. Wolaver, c 1991

4 - *IC Op Amp Cookbook* by Walter G. Jung, c 1986 (especially chapters 1, 3 & 9)

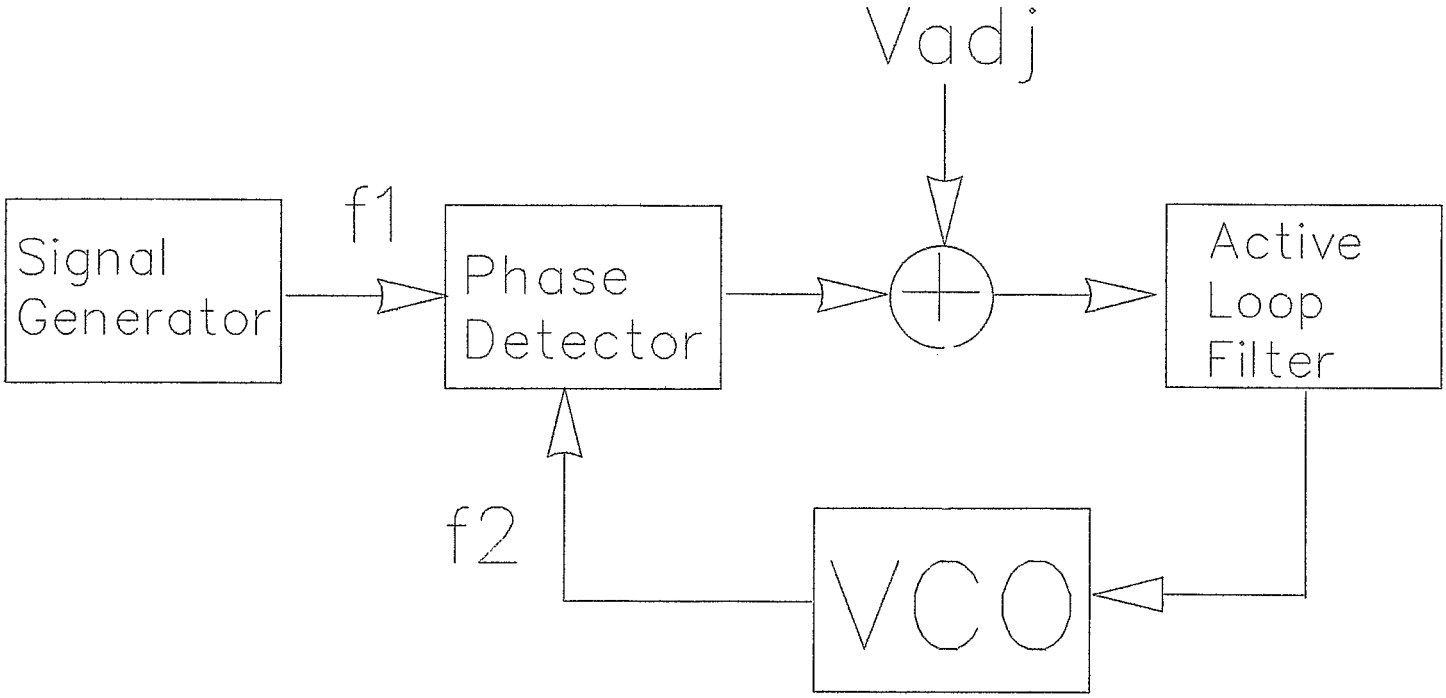


Figure 1. PLL Phase Shifter Block Diagram

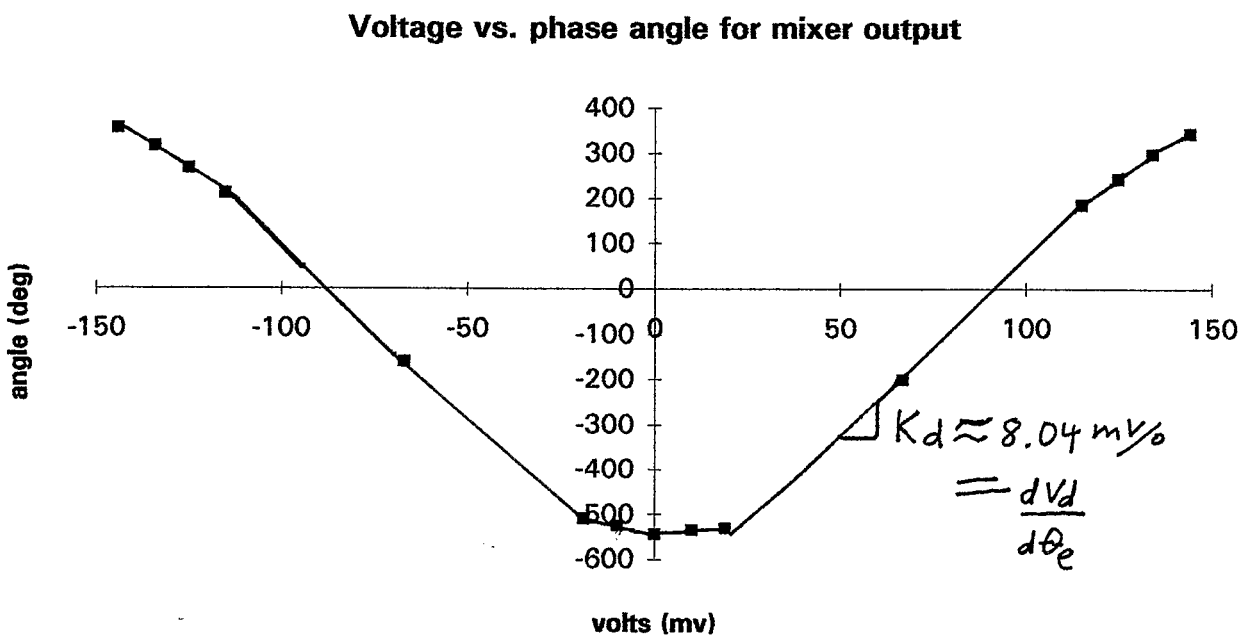
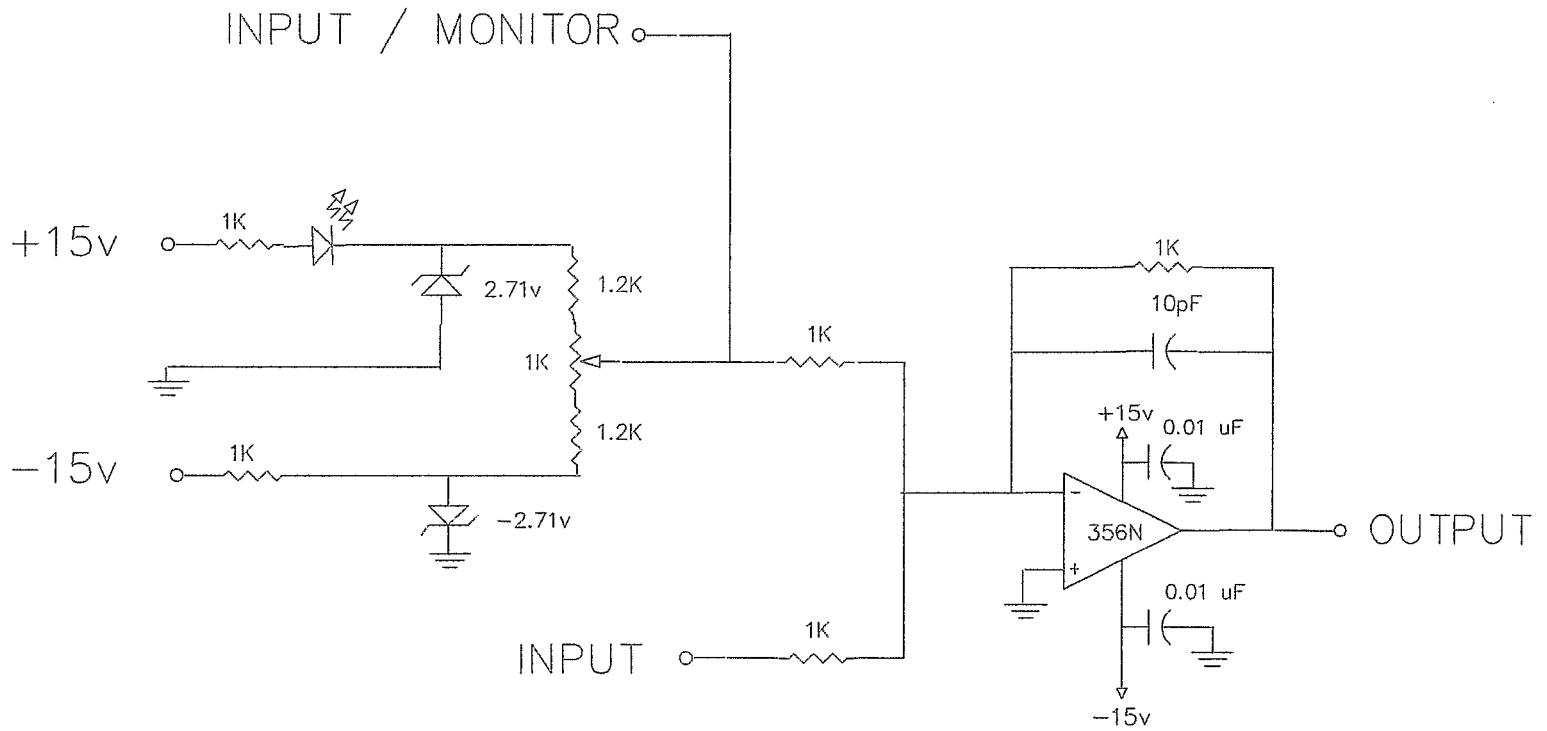
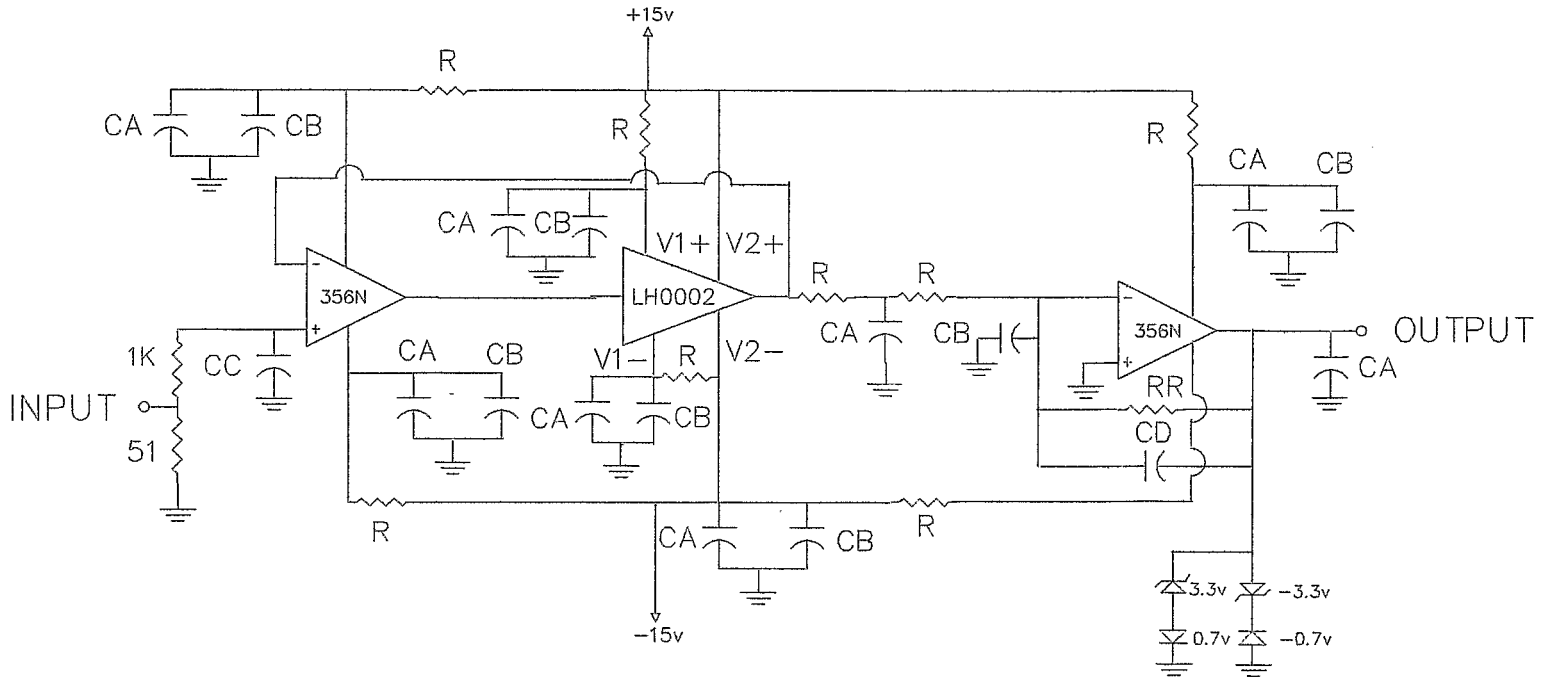


Figure 2. Phase Detector Output.



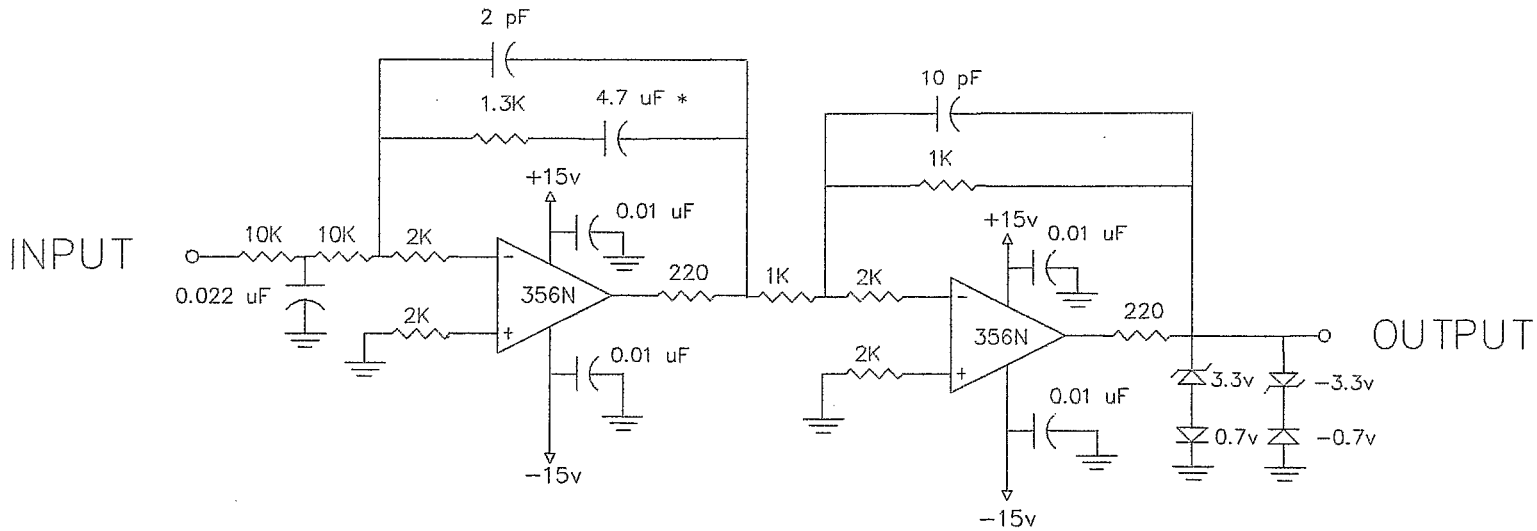
Voltage from pot:
−280 mv to +280 mv

Figure 3. Summer & Voltage Input



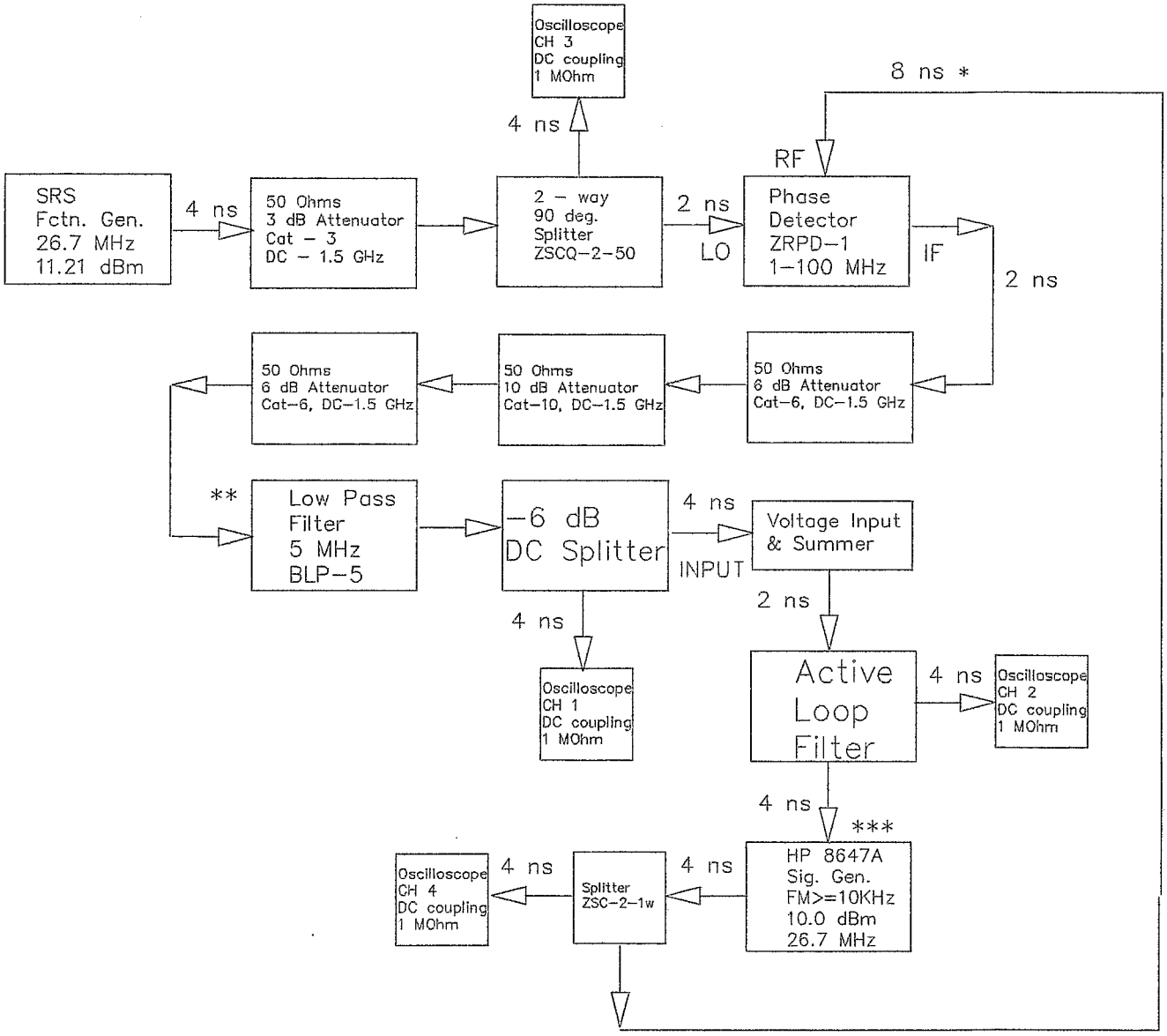
R	100 Ohms	
RR	910 KOhms	
CA	0.01 uF	Ceramic Disc
CB	1 uF	Ceramic Disc
CC	0.1 uF	Ceramic Disc
CD	4.7 uF	Tantalum

Figure 4. Bead Pull Integrator



* The capacitor used was a Tantalum, but best results are obtained with either a Teflon, polystyrene, or polypropylene capacitor.

Figure 5. Active Loop Filter



NOTE: All Attenuators, the low pass filter, & the phase detector are Mini-Circuits brand.

* Time represents the time of 50 Ohm cables for signals to propagate.

** Takes out the HF noise (@ 53 MHz).

*** FM can be as low as 500 Hz, but becomes very sensitive to the voltage inputed into the summer.

Figure 6. PLL Phase Shifter Test Set-up

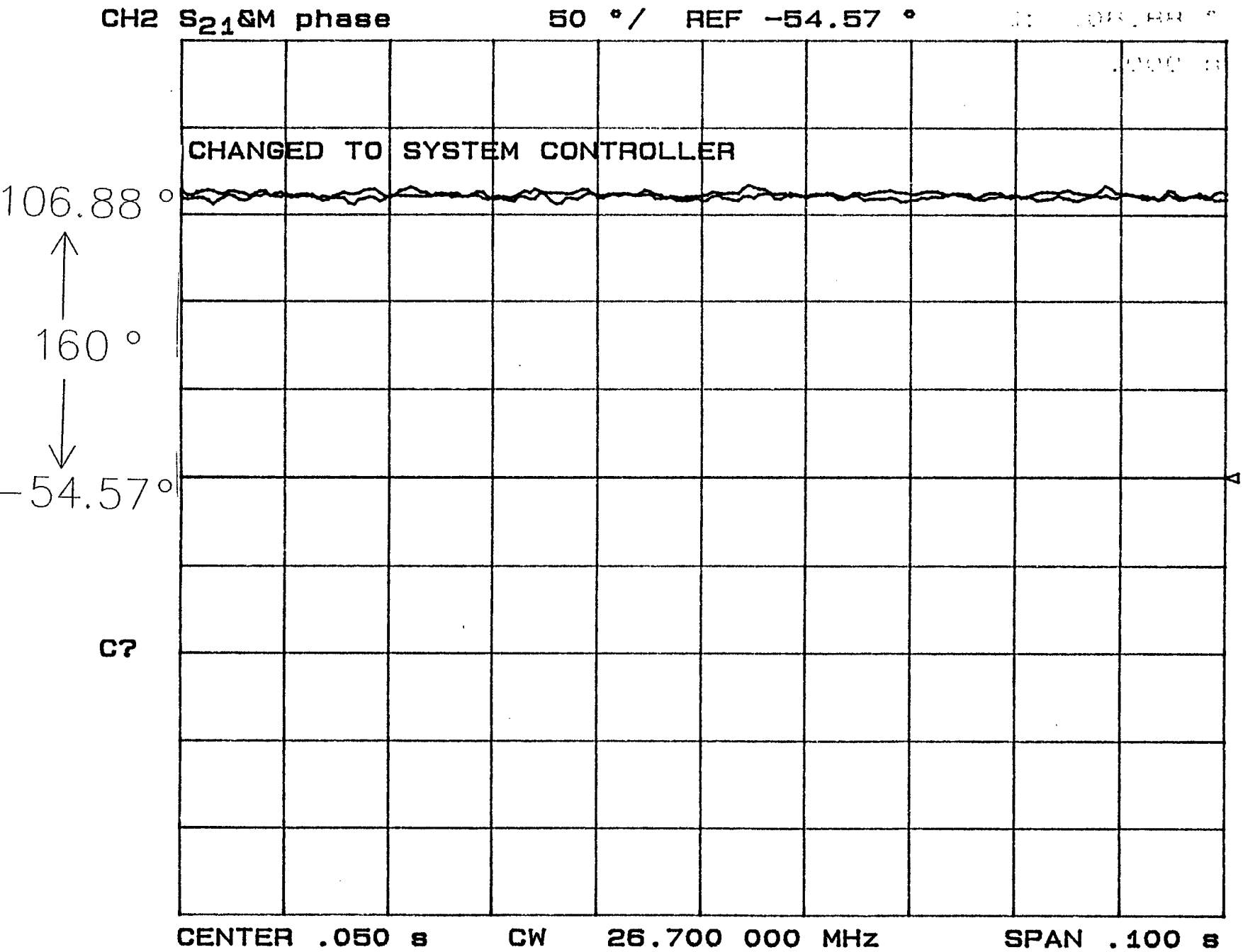

CH2 S21&M phase 50 °/ REF -54.57 °
CHANGED TO SYSTEM CONTROLLER
106.88 °
160 °
-54.57 °
C?
CENTER .050 s CW 26.700 000 MHz SPAN .100 s

Figure 7a.

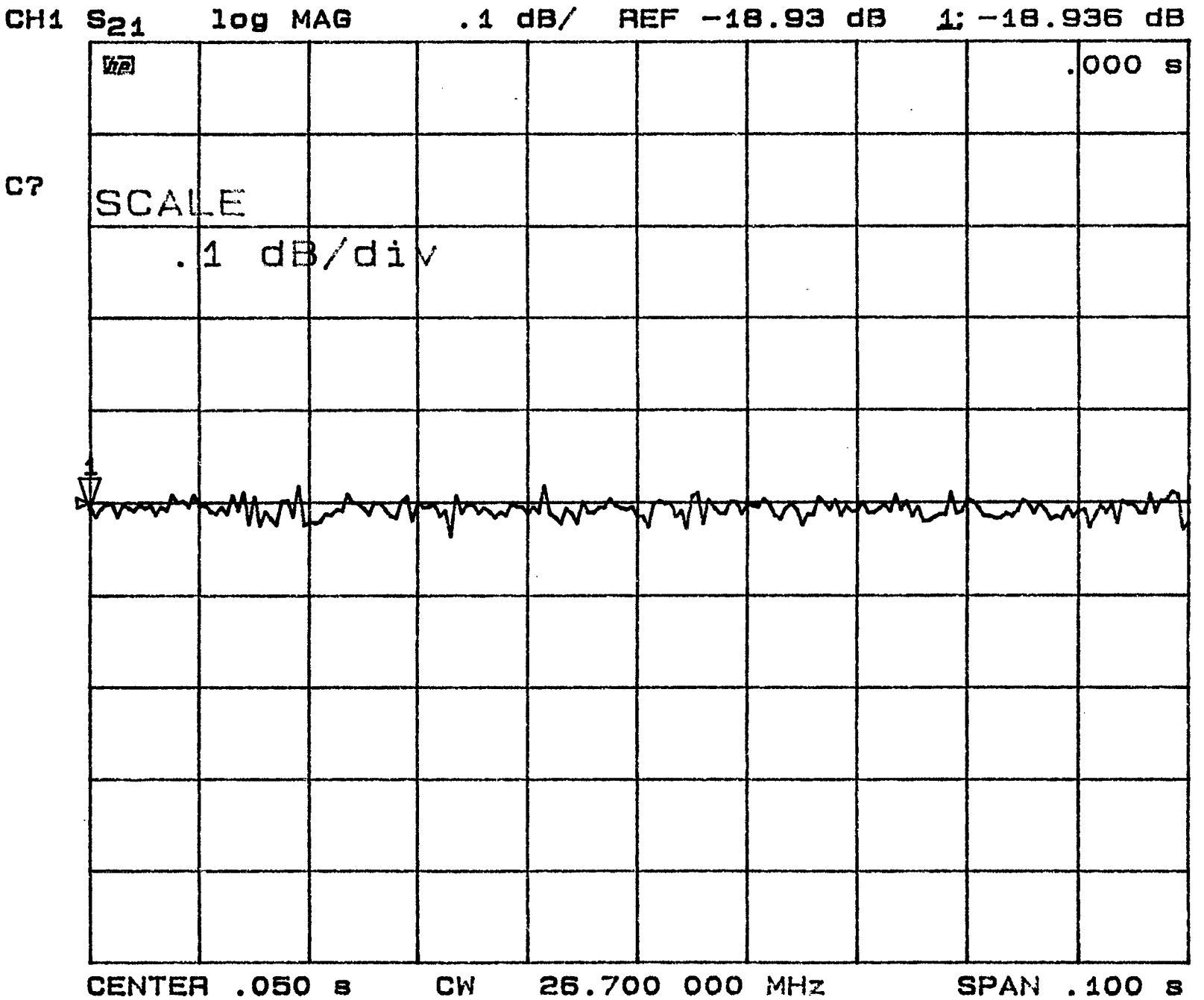

CH1 S21 log MAG .1 dB/ REF -18.93 dB 1: -18.936 dB
.000 s
C?
SCALE
.1 dB/div
1
CENTER .050 s CW 26.700 000 MHz SPAN .100 s

Figure 7b.

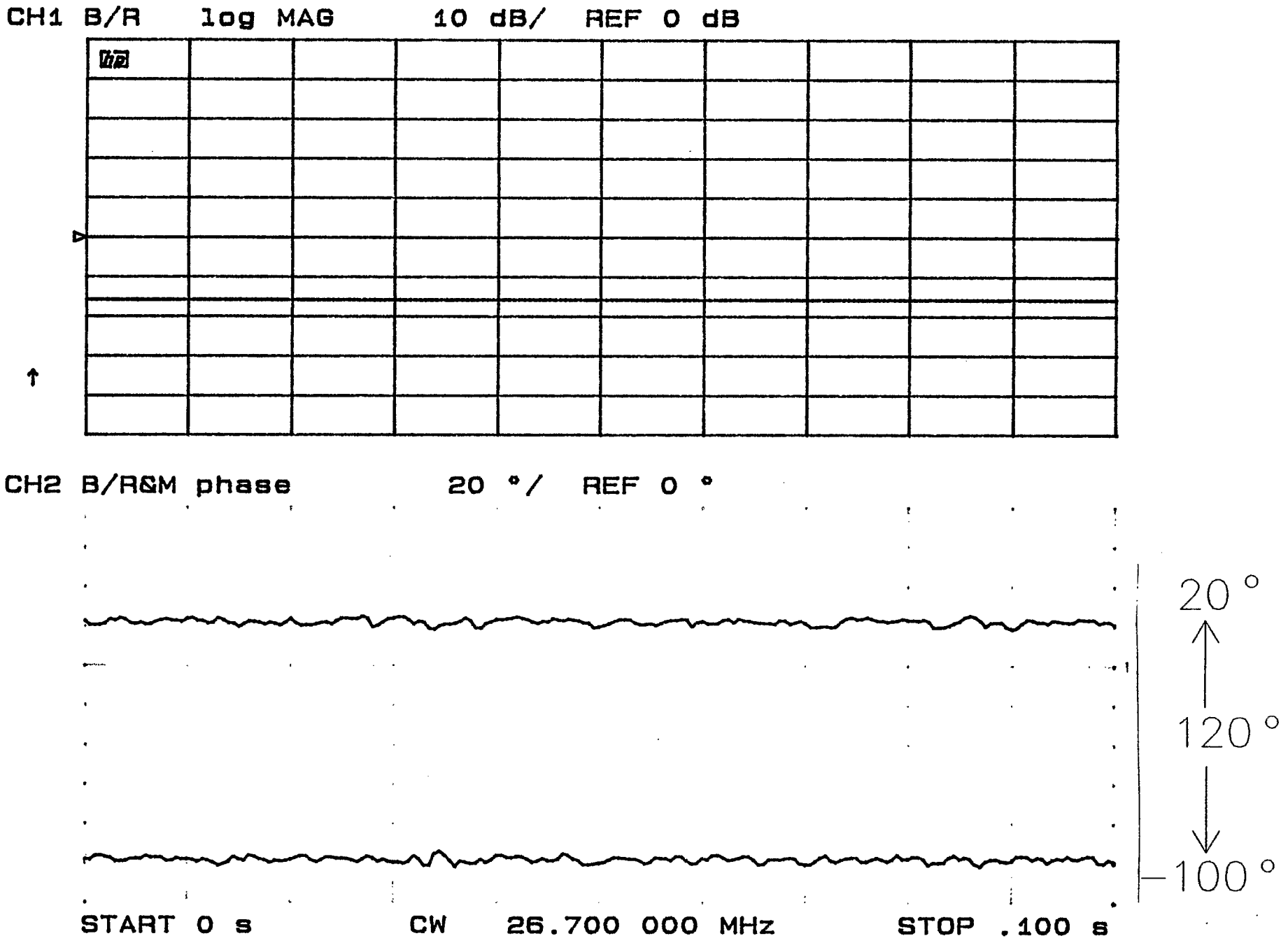

CH1 B/R log MAG 10 dB/ REF 0 dB
CH2 B/R&M phase 20 °/ REF 0 °
20 °
120 °
-100 °
START 0 s
CW 26.700 000 MHz
STOP .100 s

Figure 7c.

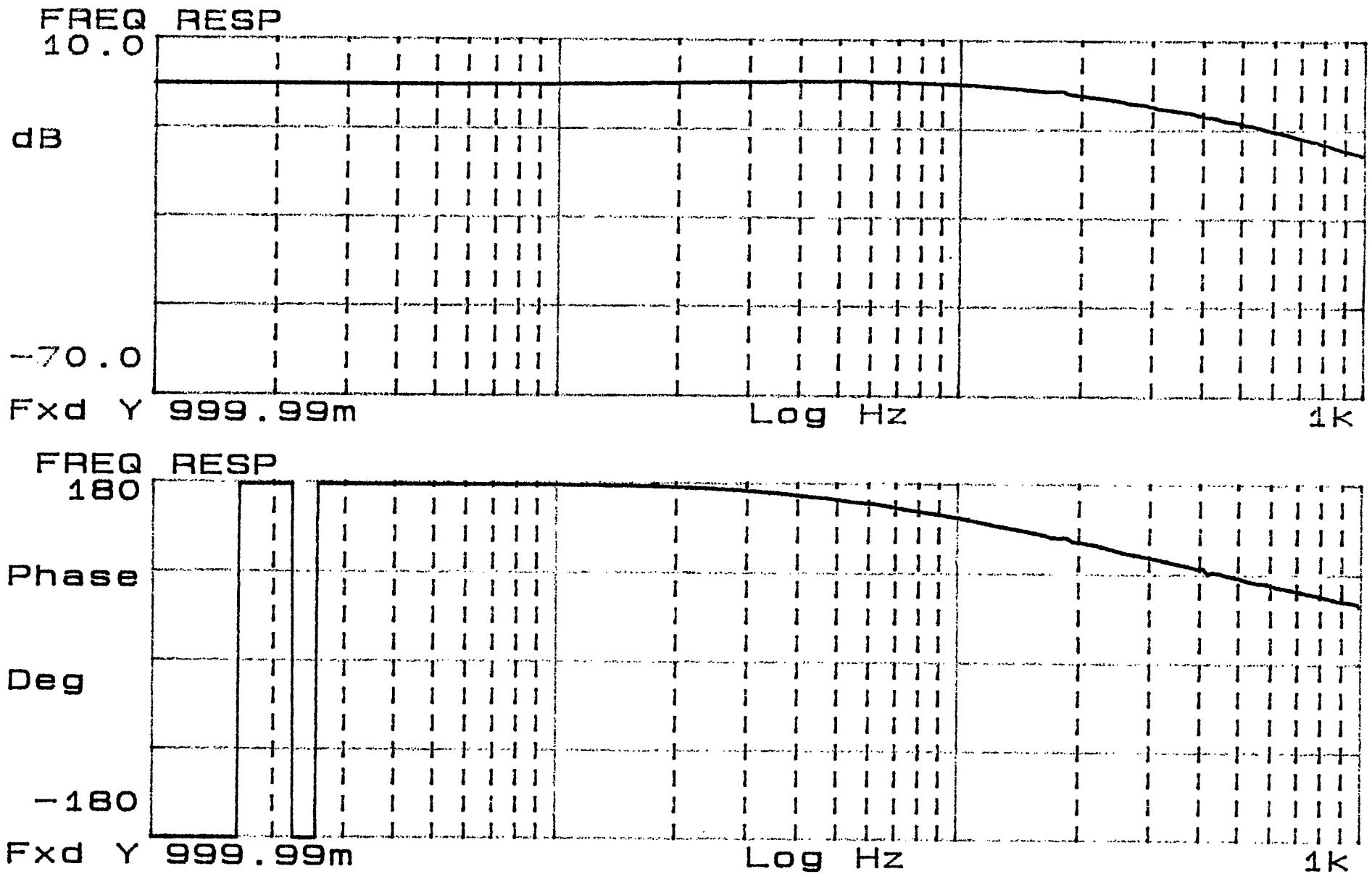

FREQ RESP
10.0
dB
-70.0
Fxd Y 999.99m
Log Hz
1k
FREQ RESP
180
Phase
Deg
-180
Fxd Y 999.99m
Log Hz
1k

Figure 8a.

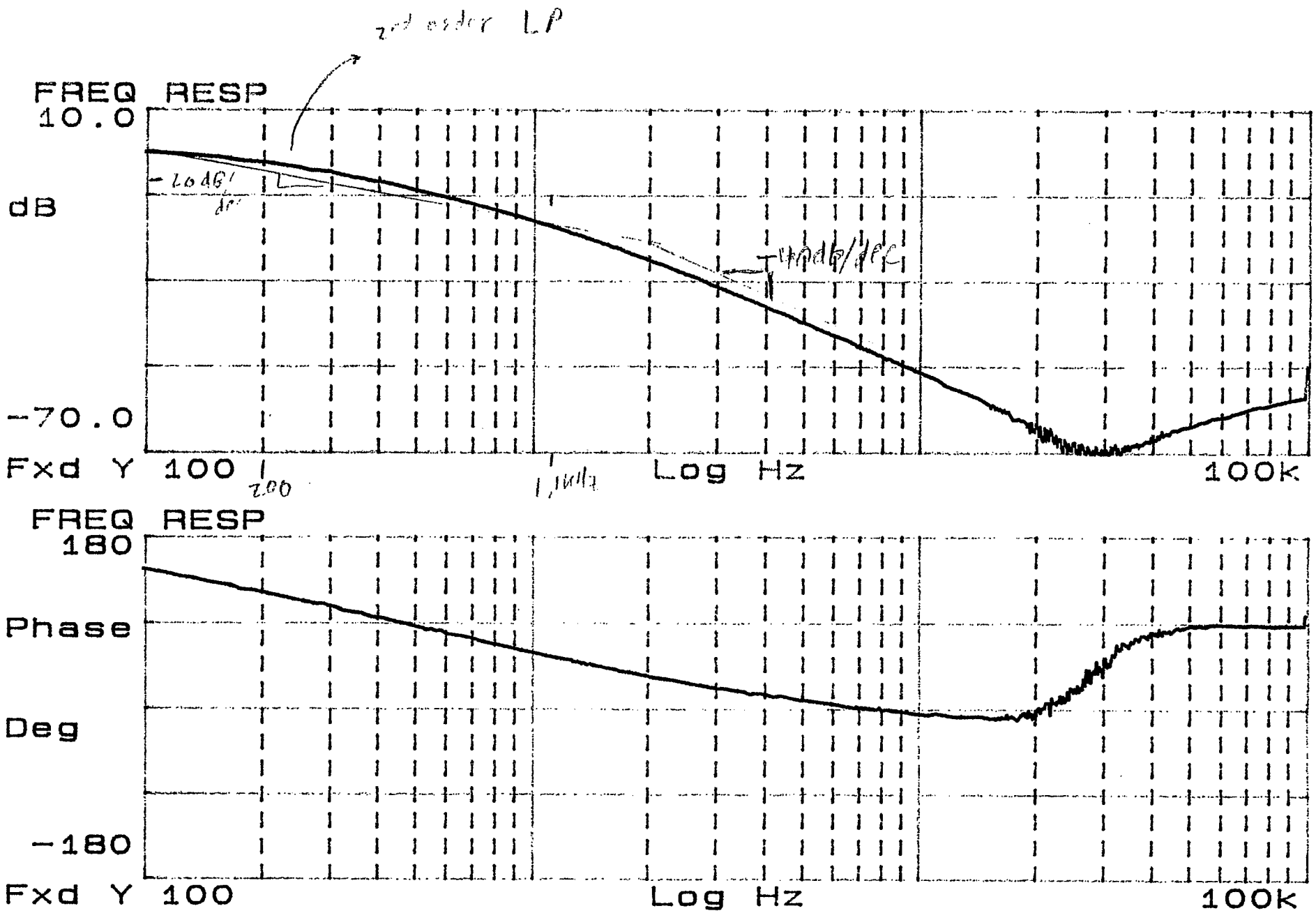

2nd order LP
FREQ RESP
10.0
dB
-70.0
Fxd Y 100
200
1,000
Log Hz
100K
FREQ RESP
180
Phase
Deg
-180
Fxd Y 100
Log Hz
100K

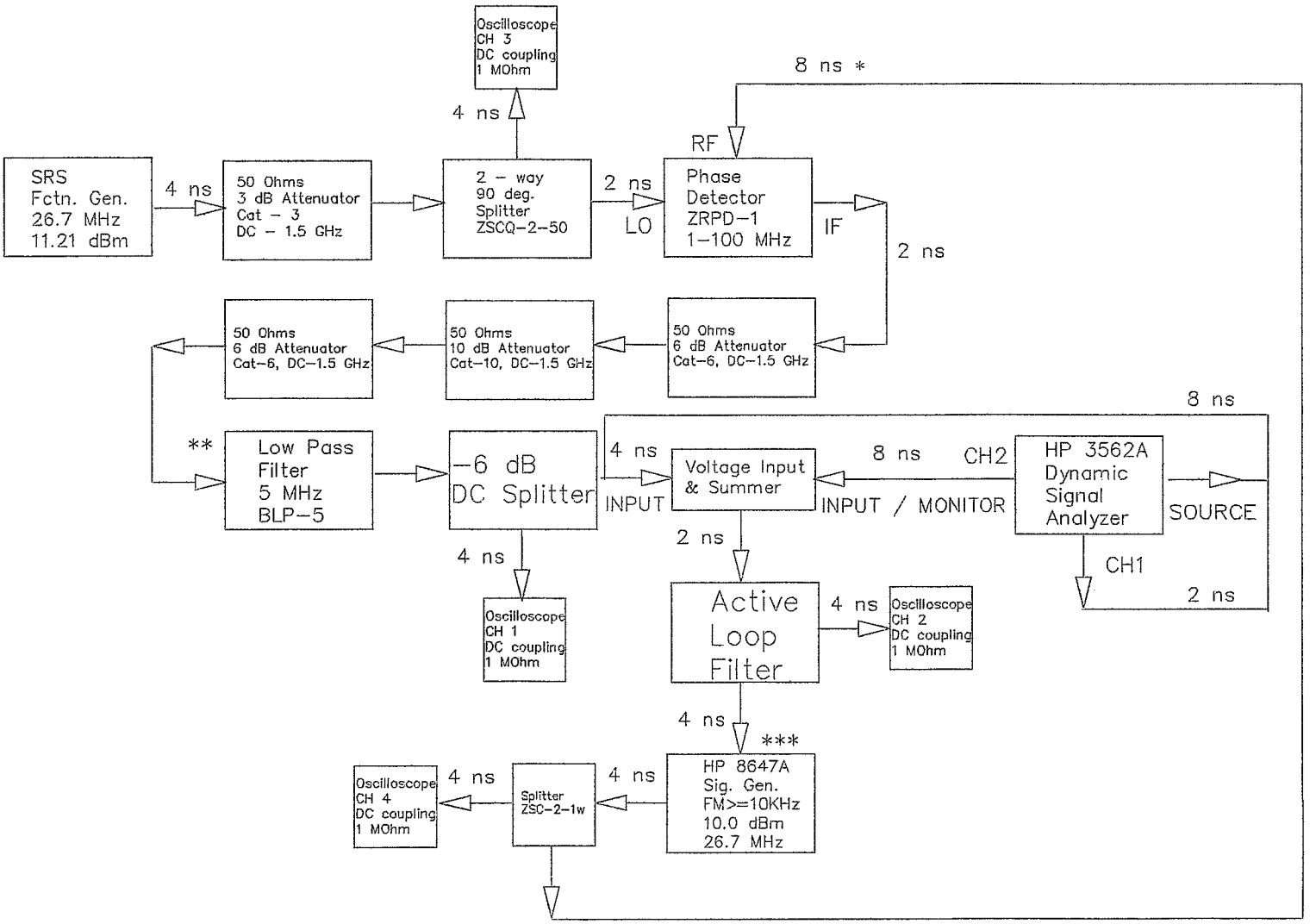
Figure 8b.

Curve Fit
Poles And Zeros

POLES 0	ZEROS 0
1 -1.12951k	-98.9308k
2 -187.048	-17.9604k
3 53.3189k±j 107.219k	17.4328k

Time delay= 0.0 S Gain= 113.3 Scale= 1.0

Figure 9.



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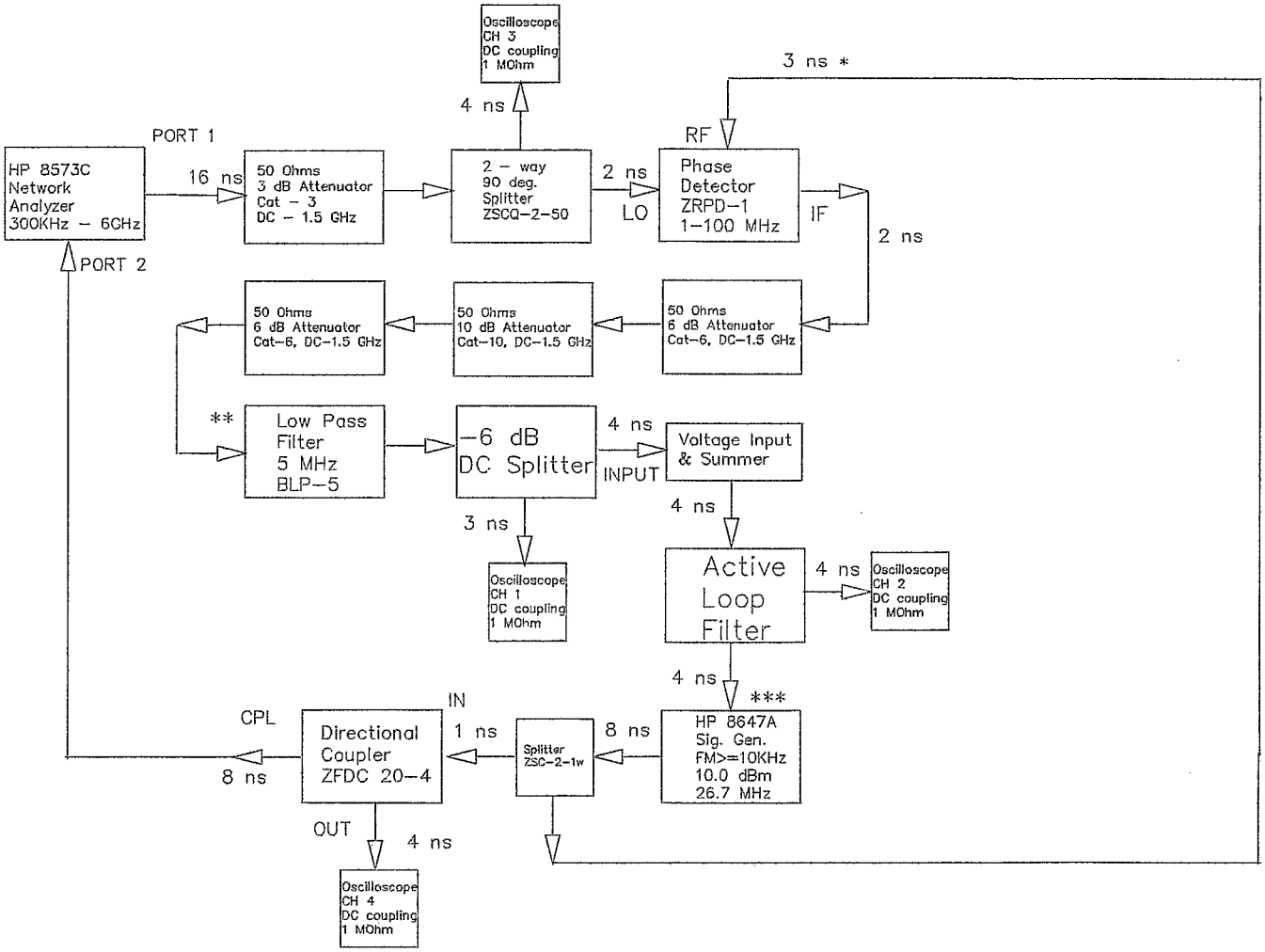
* Time represents the time of 50 Ohm cables for signals to propagate.

** Takes out the HF noise (@ 53 MHz).

*** FM can be as low as 500 Hz, but becomes very sensitive to the voltage inputed into the summer.

Figure 10. PLL Phase Shifter Test Set-up for Frequency Response



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*** FM can be as low as 500 Hz, but becomes very sensitive to the voltage inputed into the summer.

Figure 11. PLL Phase Shifter Test Set–up for Network Analyzer Measurement.