RHIC EventLink Receiver

K.Vetter

December 29, 1998

REV. 6

1.0 OVERVIEW

The EventLink Receiver is a plug-in daughter card mounted on the RHIC VME/VSB mother board. The purpose of this board is to generate an interrupt for each decoded event and place the event on the data bus for the mother board to read.

2.0 EVENTLINK INTERFACE

The purpose of this function is decode serial timeline events and generate an interrupt based on the event specified by the FEC. This function first converts the serial input data to a parallel 8-bit word. The 8-bit word is then used to address a DUAL PORT RAM (DPRAM). There are 256 unique event codes on the RHIC timeline. For each event there will be an associated entry in the DPRAM. A logic HIGH in the LSB position of the DPRAM will be used to indicated a desired Event decode. When an 8-bit event addresses an active location in the DPRAM the module will generate an interrupt. The active interrupt will latch the Event that caused the interrupt. No further timeline Events will be processed until the Event has been read, and the interrupt cleared.

NOTE: It will be the responsibility of the FEC to load the DPRAM with the desired EVENT interrupt information.

3.0 BOARD ADDRESSING

Table-2 defines the memory map for the EventLink Receiver. The EventLink can inserted into any of the four VME/VSB mother board slots with the following base addresses based on the slot. Table-1 defines the base addresses for each of the four possible slots.

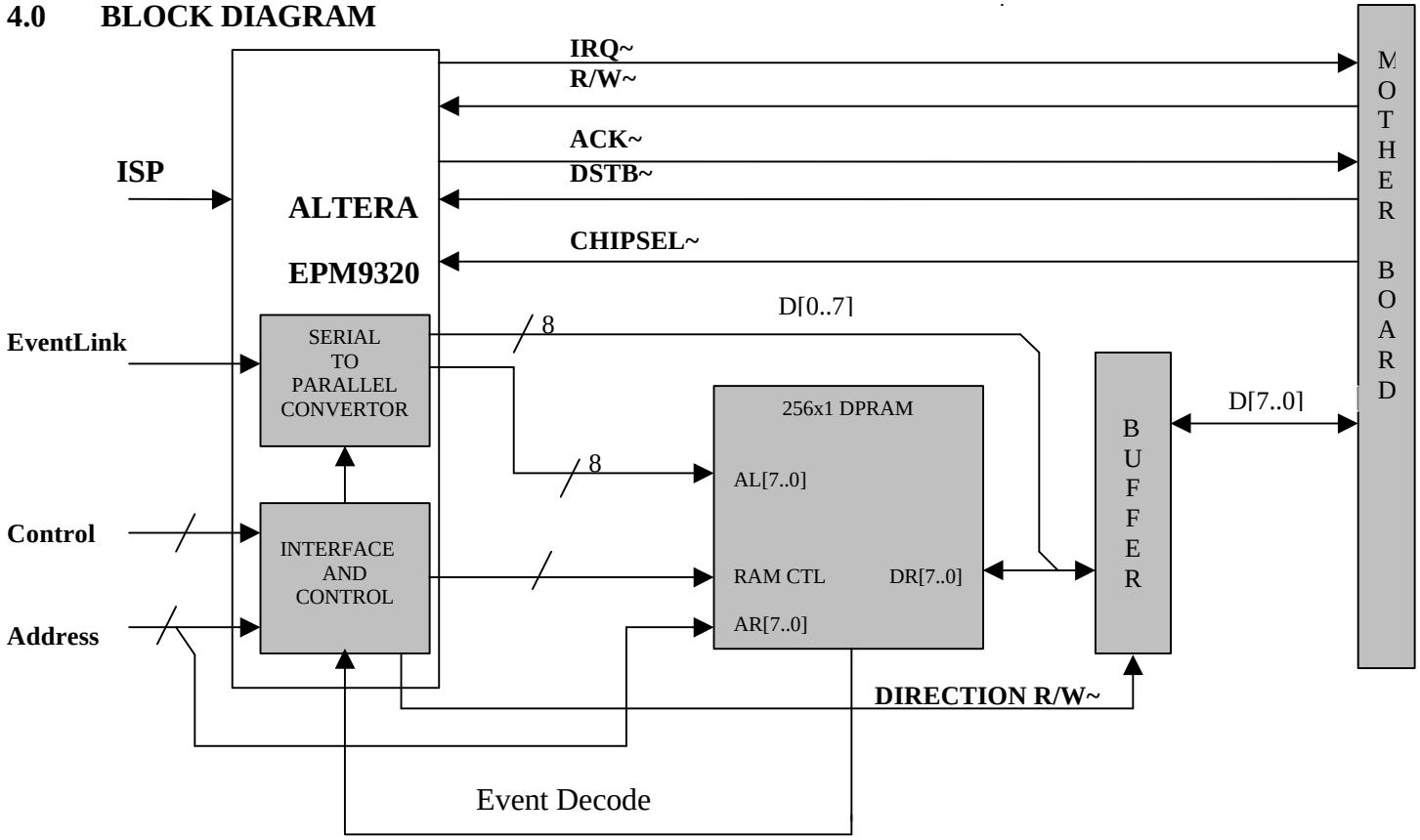
POSITION	**Base Address**
SLOT 1	0x00010000
SLOT2	0x00020000
SLOT 3	0x00030000
SLOT 4	0x00040000

Table 1

PARAMETER	ADDRESS RANGE
WRITE EVENT DECODE DPRAM	Base address + (0x00 – 0xFF)
Clear IRQ~	READ @ Base address + 0x100
Disable IRQ~	READ @ Base address + 0x101
Enable IRQ~	READ @ Base address + 0x102

Table 2

4.0 BLOCK DIAGRAM



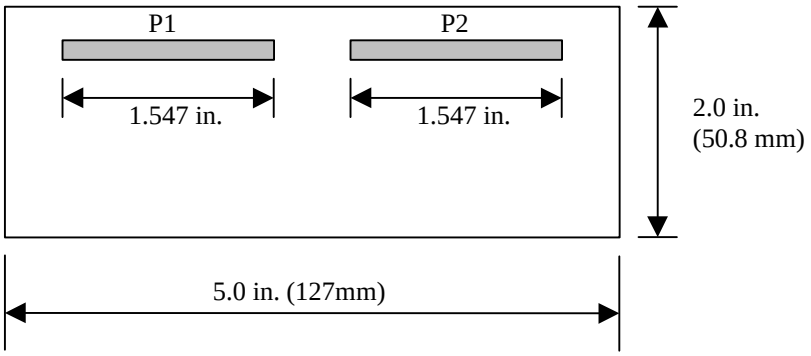
5.0 POWER REQUIREMENTS

Table-3 indicates the worst-case power requirements.

VOLTAGE	CURRENT	POWER
+5v	539 ma	2.7 watts

Table 3

6.0 MECHANICAL OUTLINE



INTERCONNECTIONS

The module will plug into the VSB mother board via a 140-PIN connector (PA). An on board ISP header (J1) has been included for independent development. System ISP will be performed by a single ISP port on the front panel of the VSB mother board in which this module plugs into. The ISP lines will connected to the mother board via the PB connector. A green LED will be mounted on the front panel of the mother board indicating EventLink activity.

CONNECTOR	PIN NUMBER	SIGNAL NAME	CHARACTERISTICS
P1	1	A0	TTL
P1	2	D0	TTL
P1	3	A1	TTL
P1	4	D1	TTL
P1	5	A2	TTL
P1	6	D2	TTL
P1	7	A3	TTL
P1	8	D3	TTL
P1	9	A4	TTL
P1	10	D4	TTL
P1	11	A5	TTL
P1	12	D5	TTL
P1	13	A6	TTL
P1	14	D6	TTL
P1	15	A7	TTL
P1	16	D7	TTL
P1	17	A8	TTL
P1	18	D8	TTL
P1	19	A9	TTL
P1	20	D9	TTL
P1	21	A10	TTL
P1	22	D10	TTL
P1	23	A11	TTL
P1	24	D11	TTL
P1	25	A12	TTL
P1	26	D12	TTL
P1	27	A13	TTL
P1	28	D13	TTL
P1	29	A14	TTL
P1	30	D14	TTL
P1	31	A15	TTL
P1	32	D15	TTL
P1	33	A16	TTL
P1	34	D16	TTL
P1	35	A17	TTL
P1	36	D17	TTL
P1	37	A18	TTL
P1	38	D18	TTL
P1	39	A19	TTL
P1	40	D19	TTL
P1	41	A20	TTL

P1	42	D20	TTL
P1	43	A21	TTL
P1	44	D21	TTL
P1	45	A22	TTL
P1	46	D22	TTL
P1	47	A23	TTL
P1	48	D23	TTL
P1	49	GND	TTL
P1	50	D24	TTL
P1	51	CHIPSEL~	TTL
P1	52	D25	TTL
P1	53	GND	POWER RETURN
P1	54	D26	TTL
P1	55	R/W~	TTL
P1	56	D27	TTL
P1	57	GND	GND
P1	58	D28	TTL
P1	59	DSTB~	TTL
P1	60	D29	TTL
P1	61	GND	GND
P1	62	D30	TTL
P1	63	ACK~	TTL
P1	64	D31	TTL
P1	65	SPARE	N/A
P1	66	GND	GND
P1	67	16 MHz CLK	TTL
P1	68	SPARE	N/A
P1	69	GND	GND
P2	1	GND	GND
P2	2	IRQ~	TTL
P2	3	SPARE	N/A
P2	4	GND	GND
P2	5	GND	GND
P2	6	+12VDC	+12VDC
P2	7	-12VDC	-12VDC
P2	8	GND	GND
P2	9	GND	GND
P2	10	+5VDC	+5VDC
P2	11	+5VDC	+5VDC
P2	12	+5VDC	+5VDC
P2	13	+5VDC	+5VDC
P2	14	NC5	TTL
P2	15	NC6	TTL
P2	16	NC1	TTL
P2	17	NC2	TTL
P2	18	SPARE	N/A
P2	19	SPARE	N/A
P2	20	SPARE	N/A
P2	21	SPARE	N/A
P2	22	SPARE	N/A

P2	23	SPARE	N/A
P2	24	SPARE	N/A
P2	25	SPARE	N/A
P2	26	SPARE	N/A
P2	27	SPARE	N/A
P2	28	SPARE	N/A
P2	29	SPARE	N/A
P2	30	SPARE	N/A
P2	31	TCK	TTL
P2	32	GND	GND
P2	33	TDO	TTL
P2	34	+5V	+5V
P2	35	TMS	TTL
P2	36	N/C	N/A
P2	37	N/C	N/A
P2	38	N/C	N/A
P2	39	TDI	TTL
P2	40	GND	GND
P2	41	SPARE	N/A
P2	42	EVENTLINK+	TTL
P2	43	EVENLINK-	TTL
P2	44	GND	GND
P2	45	+5V	+5V
P2	46	EL LED DRIVE	TTL
P2	47	GND	GND
P2	48	SPARE	N/A
P2	49	SPARE	N/A
P2	50	SPARE	N/A
P2	51	SPARE	N/A
P2	52	SPARE	N/A
P2	53	SPARE	N/A
P2	54	SPARE	N/A
P2	55	SPARE	N/A
P2	56	SPARE	N/A
P2	57	SPARE	N/A
P2	58	SPARE	N/A
P2	59	SPARE	N/A
P2	60	SPARE	N/A
P2	61	SPARE	N/A
P2	62	SPARE	N/A
P2	63	SPARE	N/A
P2	64	SPARE	N/A
P2	65	SPARE	N/A
P2	66	SPARE	N/A
P2	67	SPARE	N/A
P2	68	SPARE	N/A
P2	69	SPARE	N/A

J1	1	TCK	TTL
J1	2	GND	GND
J1	3	TDO	TTL
J1	4	+5V	+5V
J1	5	TMS	TTL
J1	6	N/C	N/A
J1	7	N/C	N/A
J1	8	N/C	N/A
J1	9	TDI	TTL
J1	10	GND	GND